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The Origins of Intel's New Transistor, and Its Future

A Q&A with Chenming Hu, coinventor of both the FinFET and its likely competitor

By RACHEL COURTLAND / MAY 2011



Photo: Peg Skorpinski

9 May 2011—Last Wednesday, Intel announced a [big change](#) to the electronic switches at the heart of its CPUs. Going forward, the firm will be using three-dimensional transistors to take the place of long-used planar devices.

The new transistors—dubbed "tri-gates"—are a variation on the [FinFET](#), a transistor design that substitutes the flat channel through which electrons flow with a 3-D ridge, or fin. Popping the channel out of plane and draping the gate—which switches the transistor on and off—over it will allow Intel to shrink the smallest features in its transistors from 32 nanometers to 22 nm while cutting power consumption in half. This feat would be impossible to do with the transistor design the company had been using.

How did this 3-D design win its way into production? We asked the coinventor of the FinFET, IEEE Fellow [Chenming Hu](#), a professor emeritus at the University of California, Berkeley, how the new transistors got their start, why we need them now, and where they will go from here.

IEEE Spectrum: We've been shrinking two-dimensional, or planar, transistors just fine for 50 years. Why are we seeing a switch to three-

dimensional FinFETs?

Chenming Hu: I'll distill the problem with planar transistors to a single point. It all stems from the fact that it is very difficult to turn off a transistor when it's very small. In other words, you can't stop the current flowing through the transistor when you don't want the current to flow.

I'll use an analogy to explain this. There is a garden hose lying on a soggy lawn, and you want to stop the water from flowing into this lawn. If there's a long hose, you can call your friends to come in and put 10 pairs of hands down, and you can stop the water. Now imagine you shorten the hose so you cannot even put one palm on it to stop it. Now you shorten it even more, so you can only put one finger on it. It's impossible to stop.

In the past 10 years, people have dealt with this garden hose problem in various ways, and one way has been to sacrifice power. For 250-nm transistors, the power-supply voltage was 2.5 volts; for 180 nm, it was 1.8 V; for 130 nm, it was 1.3 V. The pattern was very regular until 90 nm, but it reached a limit. Instead of 0.9 V, you know what the industry used? 1.2 V. Even at 45 nm, the industry still used 0.9 V instead of 0.45 V.

IEEE Spectrum: So current is leaking even when the transistors are off. To get around that problem, you have to use a higher voltage to make the difference between on and off more obvious?

Chenming Hu: Exactly. What's the consequence of that? Power is proportional to the square of the voltage. So if you use twice as high a voltage as the historical trend, your cellphone will consume four times the power. The pain is just too big to keep going that way. We thought planar technology would run out of steam sometime after 25 nm, and it did.

IEEE Spectrum: How do FinFETs help fix the leaky garden hose problem?

Chenming Hu: Remember, the hose is on a soggy, soft lawn. So what if instead of pressing your finger on this garden hose, you pinch your fingers on the two sides of the garden hose? That's the analogy. The weak point, the soggy lawn,

is the silicon substrate. So you really have to do something on both sides so you're pinching against something firm, and that's what the FinFET is doing. We should pinch the channel [where electrons flow] on two sides and on top. The more pinching sides, the better.

Pinching the hose will allow us to use a much, much shorter hose. That's extremely important. Making things small is really the key of making the electronics cheaper, faster, and lower power.

IEEE Spectrum: The idea for FinFETs has been around for a while. How did it all get started?

Chenming Hu: DARPA [the Defense Advanced Research Projects Agency] sent out a request for proposals in 1996 for ideas to develop electronic switches beyond 25 nm. At the time, the industry was using 250-nm transistors, and the general view was that transistors could not be scaled below 100 nm. But my students and I had already been thinking about how to get transistors to scale to 25 nm and beyond.

There was a quick meeting probably lasting only five minutes between myself and two colleagues—Professor [Tsu-Jae King Liu](#) and Professor [Jeff Bokor](#). The meeting was short because we already knew what to do.

I was on a flight to a conference in Japan, and I had about 10 hours, so I just wrote down the technical proposal in longhand. I proposed two structures that we'd been thinking about for a while. One was FinFETs, and the other is what we call an ultrathin-body silicon-on-insulator (UTB SOI).

We got the contract in 1997, and that gave us the resources to demonstrate FinFETs experimentally. A young graduate student named Xuejue "Cathy" Huang made the working device, and the team of three professors and 11 students and visiting researchers [published it in 1999](#).

IEEE Spectrum: How did the industry react to the FinFET paper?

Chenming Hu: It was an instant hit. I remember Cathy and I were invited to Intel Santa Clara just a couple of months after the publication, and in that same year, 2000, I was invited to Intel Oregon twice. At the time, people were asking me how long it would take for the idea to get into production. I said about 10 years, so I guess I was off by one.

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