system is slightly over-sized, so that through the year it produces 10 percent more power than can be used at the site. The utilization factor would be 0.90 in this case. Let us now consider two different utility buy-back policies, assuming for simplicity that the retail price of utility power just equals that of power from a PV system. If the utility were to buy power at only 50 percent of the retail price it charges, the utilization factor would be 0.95. If instead the excess power were produced at times of peak demand when the utility was paying 1.2 times its average retail price for electricity fed back to the grid, the utilization factor would become 1.02 (10 percent of power fed back at a 20 percent premium price). Thus the result of buy-back at this peak rate would be to lower the price of the PV power by from 7 percent (compared with 50 percent buy-back price) to 13 percent (compared with wasting the 10 percent excess power).

8.3 UTILITY ISSUES IN INDUSTRIALIZED COUNTRIES

Devoted proponents of solar energy may want to cut their ties to the utilities and "go it alone" when PV systems are available at costs somewhat lower than today's. Most people will likely choose to retain their utility connection, however, buying less energy than before and enjoying the benefits of system stability, backup power during periods of little insolation, and the sale of power to the utility when the solar units are producing more than is needed. It is important, therefore, to consider the issues that on-site PV systems will raise for the utilities.

To condense the vast amount of material on this topic we shall describe a possible scenario as it might be played in 1986 and beyond. The reader interested in more detail should start with the OTA (1978) volumes and the many references they contain on technical, economic, and legal issues involving utilities and on-site equipment.

Hypothetical Scenario for a PV-Powered Future

Let us assume that because of developments around the world, the DOE price goals for both solar cells and for BOS costs have been met. What might be the typical relationship between the utility and the resident of a building fitted with a PV system? What is the likely attitude of the utility regarding the increasing number of such on-site systems? What problems are likely to arise? Answers have been suggested by studies made by industry, government, and by the utilities themselves or their collective industry research organizations, such as the Electric Power Research Institute (EPRI) in the United States. Here is what we might see when the price goals have been met and on-site PV equipment is readily obtainable.

Since the reactions of those utilities that examined PV power by the early 1980s were generally positive, we find that the utilities welcome the growth of these on-site facilities. The standardized modular PV systems can be installed quickly, permitting the generating capacity to grow rapidly in response to increasing demand. The on-site systems are controlled by the utility, through signals sent over the grid to inexpensive electronic controllers at each site. This centralized control permits the utility to minimize the cost of backup energy supplied, since the utility alone can be aware of and responsive to the *marginal* cost of electricity. There are several different pricing schemes in use, having been gradually introduced around the world since the 1970s. Time-of-day pricing makes electricity furnished during times of peak demand more expensive than off-peak electricity, to reflect the higher cost of providing intermediate and peak-load power from diesel-driven generators. Control of appliances and equipment using large amounts of energy is lodged in the utility control room, from which the utility can transmit a signal over the electricity-distribution system to activate electronic switches at each customer's site. The resident may manually override this control, which can turn off electric clothes dryers and water-heating equipment, but the override option is seldom exercised because residents find that postponing the washing and heating can greatly reduce the utility bills. Water heated during off-peak hours is stored in well-insulated tanks for later use, as was being done already in the 1970s in residences in many European countries. Individuals who want still lower rates may opt for truly *interruptible* service, in which delivery of power from the utility can be terminated entirely for hours during periods of short supply.

In return for these additional system complexities, the utility has a demand curve that is considerably smoother than those typical of earlier times, so that large, efficient central baseload plants can generate a greater fraction of the utility power at low cost. In contrast with the strategy used by the operator of a typical stand-alone PV system, the utility does not store the electricity generated during most sunny hours, but instead distributes it to other users on the system. The excess PV-generated power supplied to the utility on weekends when the demand is low is stored in large load-leveling and peak-shaving storage batteries owned by the utility and located near the load centers to reduce distribution losses.

Consistent with the finding in the 1970s with windpowered generators was the observation that on-site PV generators feeding power back onto the grid do not cause problems because of transients or harmonics. No system stability problems arise even when 20 or 30 percent of the power on the grid comes from on-site PV generators. It had been feared that during system outages the supposedly dead grid wires might actually have thousands of volts across them because of on-site power flowing backward through what are normally step-*down* transformers. This hazard was eliminated simply by

including an automatic cutoff switch at each site to open the connection to the utility when the central source ceased to function.

Credit for selling power back in some localities where the buy-back rate equals the rate at which electricity is sold requires no additional equipment since the ordinary integrating watt-hour meter runs either forward or backward and so registers the difference between the power received and that supplied. In other localities, a differential pricing scheme tied to time of day is in effect. An inexpensive electronic device registers the usage at the correct rate, totals the amount, and then, upon being interrogated electronically, transmits to the utility the information needed for billing.

Most consumers prefer to have the utility own and maintain the on-site equipment since they feel that raising the capital to buy the equipment outright is more burdensome than paying periodically to use utility-owned equipment—and to their surprise they find that study shows that the cost of the power produced is not materially different.

Whether events develop generally as outlined in this scenario depends upon technological development, and on the individual decisions and perceptions of literally millions of people. There appear to be no institutional, legal, or resource barriers that will prevent its becoming reality. The ultimate outcome depends on the achievable costs of the solar cell modules and the balance-of-system components.

8.4 ISSUES IN DEVELOPING COUNTRIES

On-site PV systems should be ideal for the developing nations where electric utility grids hardly exist. The systems are small and far less expensive to purchase than large central power stations, and they begin producing power within days or weeks after the start of their construction. The modularity of PV systems permits gradual, easily managed expansion as demand grows. The installations do not require imported fuel that must be transported long distances and whose price is subject to unpredictable increases. Thus the country is not required to commit itself to a form of energy production it may not be able to sustain because of increases in fuel prices, and this fact should encourage banks to loan money for PV systems.

The potential market in developing countries is huge, as there are more than 500 million people living in villages without any electric power. Life in these villages would be improved by the installation of even a small local generating system—an improvement that might reduce the drive for migration to crowded large cities in the often disappointing search for better conditions. A backup power source might not be needed in applications such as water pumping; if a backup source is required, it might be a diesel generator used only a few days each year and so requiring very little fuel.

Manufacture of some PV arrays could be done within many of the developing nations, possibly with unskilled labor and simply equipment. Because the cost of electricity in many parts of the world is several times higher than that in the industrialized nations, economic feasibility of PV systems will occur first in the developing nations as PV costs fall. Manufacturers might thus find that the market for PV technology—finished systems and manufacturing facilities—matures earliest in the developing countries and helps to support the growth of facilities for supplying photovoltaics to the industrialized nations.

8.5 SUMMARY

Solar cell systems will first compete economically at locations where the cost of conventionally produced electricity is highest—at remote locations, and at the load end of power-transmission systems. The levelized cost of PV power is sensitive to the consumer's financial and power-usage characteristics. Tax incentives and favorable utility buyback policies can greatly reduce the cost of PV-produced power. Studies show that PV power will be cheaper than conventionally produced power in the United States in the mid-1980s, provided the DOE cost goals for cells *and* balance-of-system components are met.

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PROBLEMS

8.1 *PV-powered auto* How long could a 25-hp vehicle operate on the electrical energy produced in a 24-h period by a 15 percent efficient PV system? (Assume

insolation averages 200 W/m^2, the collector area is 1 × 4 m^2, and the motor-battery total efficiency is 70 percent.)

8.2 *Levelized cost* What is the levelized cost of electricity over a 20-yr period if the cost inflates from its initial value of 4¢/kWh at an 8 percent annual rate?

8.3 *Financial incentives* Identify what factors in Eq. (8.1.1) each of the financial incentives in Table 8.4 affects.

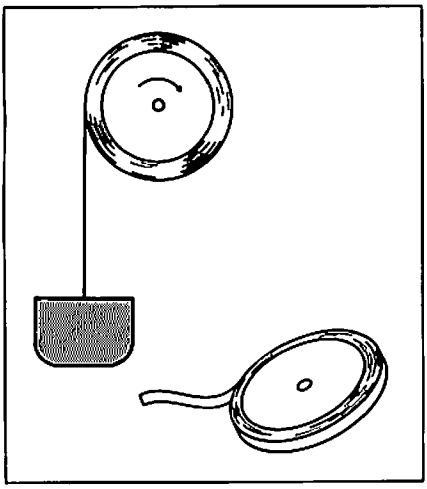
8.4 *Factors affecting economic viability* Examine some of the factors affecting economic viability of PV-generated electricity in your area. Is annual insolation high, average, or low? Is cost of utility-supplied electricity high, average, or low? If it is high or low, what factors account for this? Is time-of-day pricing in effect in your area? Do any of your major electrical energy demands occur when insolation is highest? (Air conditioning for comfort is an example for which energy storage and its associated cost may be avoided.) Does your electric utility have an energy buy-back policy? At what rates? Are area-related costs unusually high or low where you are?

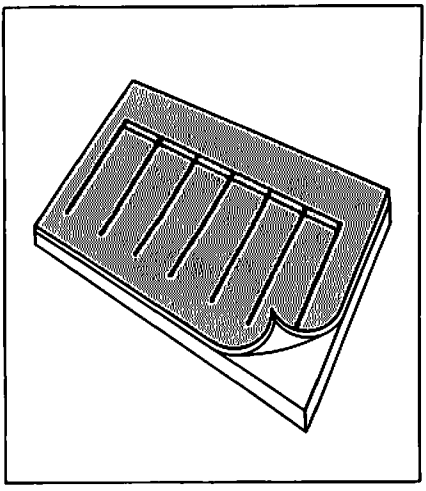
CHAPTER NINE
ADVANCED MATERIAL PREPARATION AND PROCESSING TECHNIQUES

Forming and processing thin self-supporting semiconductor sheets for low-cost, high volume manufacture of cells

CHAPTER TEN
THIN-FILM AND UNCONVENTIONAL CELL MATERIALS

Low-cost cells from amorphous and evaporated semiconductors, and thin films formed on temporary substrates





PART

THREE

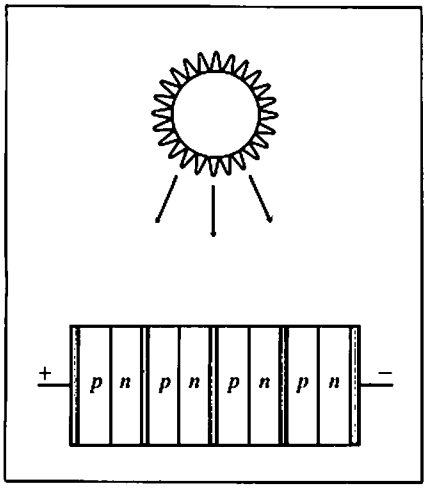
SOLAR CELL IMPROVEMENTS

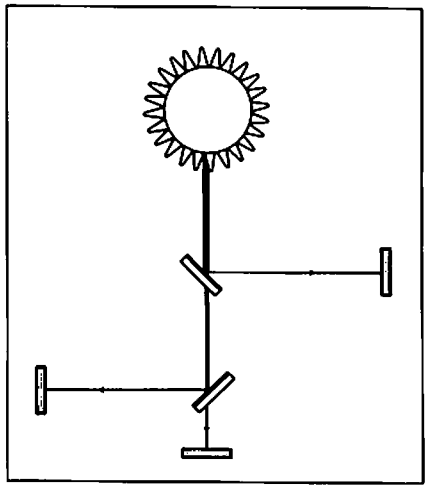
CHAPTER ELEVEN
VARIATIONS IN CELL STRUCTURE

Multiple junction and other novel cell structures mostly for high efficiency

CHAPTER TWELVE
UNCONVENTIONAL CELL SYSTEMS

Cells employing photochemistry for energy storage, novel spectral manipulations for high efficiency, and the solar power satellite



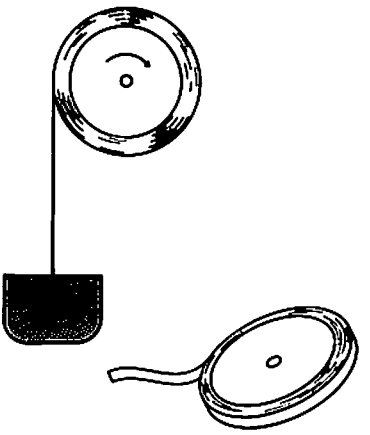


CHAPTER

NINE

ADVANCED CELL PROCESSING TECHNIQUES

CHAPTER OUTLINE



The motivations for investigating new cell processing techniques are reducing cell costs, increasing rates of cell production, and reducing the energy used in cell manufacture.

Conventional silicon cells have been made by separate and distinct manufacturing steps, as described in Chap. 4: growing the single-crystal semiconductor, cutting it into wafers, doping the wafers, forming contacts, and assembling entire arrays. With the newer fabrication methods, the demarcations between processes are blurred, as suggested by Fig. 9.1. The principal question to ask about the newer processes is, "What cell efficiency can be achieved?" The loss of carriers at imperfections in the cell material made by these methods is generally greater than in conventional cells, so the efficiency is usually lower. One must decide whether the advantages of lower cost and higher production rate compensate adequately for the lower efficiency.

In this chapter we describe promising new processes for making solar cells. These methods are grouped as follows: growing thin self-supporting semiconductor ribbons and sheets that do not require wafering; forming a semiconductor layer on a substrate; using ion implantation, lasers, and electron beams for doping, annealing, and stimulating grain growth; and achieving high optical transmission, putting on contacts, and encapsulating cells. Before discussing these topics we consider some general principles about solidification and defects in crystals, as these topics are particularly relevant in the newer methods of making cells. We conclude the chapter with a description of a hypothetical automated solar cell factory.

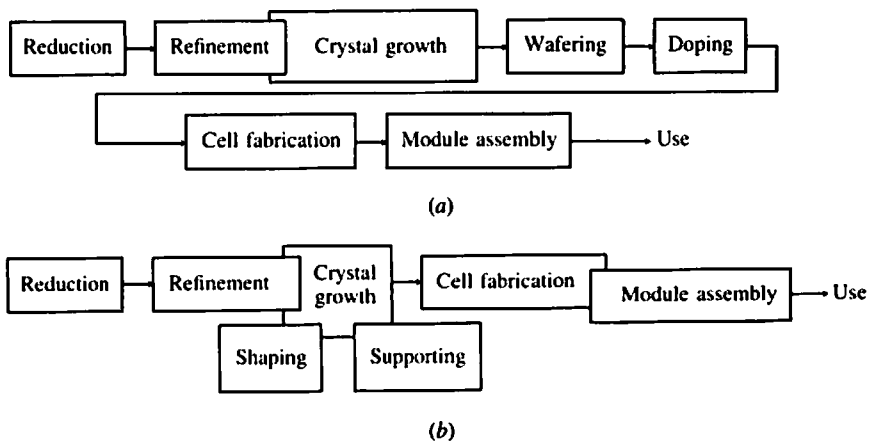


Figure 9.1 Conventional (*a*) and advanced cell processing (*b*). Some of the individual steps of conventional processing occur in a single step in the advanced processes, of which silicon ribbon growth and forming cadmium sulfide cells on float glass are examples.

9.1 SOLIDIFICATION AND THERMAL ACTIVATION

Solidification

The most common way of forming a solid is to freeze a molten mass of the material. When a molten elemental metal or semiconductor cools slowly, its temperature changes with time as shown by curve *A* in Fig. 9.2. The temperature falls until it reaches a definite value called the *freezing temperature* for that material, at which it remains for some time before beginning to fall again. At the freezing temperature, if heat is being removed from the volume rapidly, freezing will occur simultaneously at many different places in the liquid volume. Nuclei of solidifying material that reach a critical size will continue to grow as more atoms attach themselves. The latent heat given off in the freezing process flows to the melt, permitting it to remain at a constant temperature in spite of the removal of heat from its boundaries. The individual nuclei eventually become large enough to contact each other, forming a polycrystalline solid with grain boundaries.

Very different conditions are used when one makes large single crystals: A seed crystal is placed in contact with the melt for orientation, cooling is slow, and a thermal gradient is established between the melt and the solid at whose surface atoms are attaching themselves.

In a two-component melt in which both constituents are soluble in the liquid but insoluble in the solid that forms, one can show from the Gibbs phase rule that the cooling curve will have the form of curve *B* of Fig. 9.2. One of the atomic components begins to freeze out first, robbing the liquid phase of that component and changing the composition of the melt as the temperature continues to fall.

Thermal Activation

In the solidification processes that result in nearly perfect single crystals, atoms arriving at the surface of the growing solid must be able to reach the proper locations to continue the regular crystal structure. In a number of

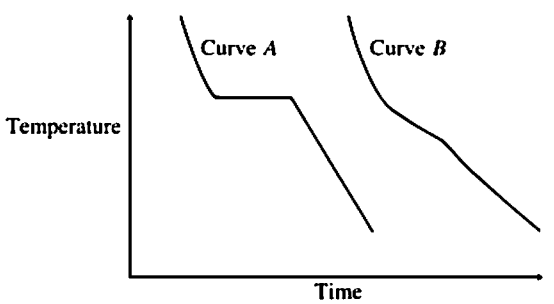


Figure 9.2 Cooling curves for an elemental solid (*A*) and for a compound solid (*B*).

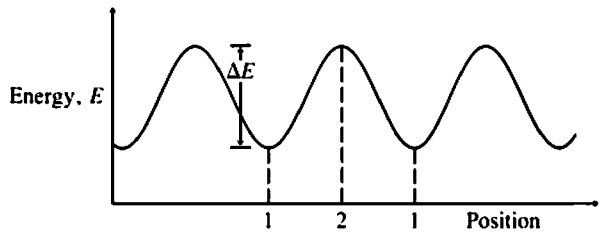


Figure 9.3 Energy of atom as a function of position in a regular crystalline solid, assumed one-dimensional for clarity.

processes that appear important for the next generation of low-cost solar cells, thermal energy is supplied to permit atoms to move to the crystallographically correct locations.

As examples, consider the growth of a layer of crystalline semiconductor upon another crystalline semiconductor. If the underlying semiconductor (A) and the semiconductor that is to form the layer (B) have the same crystal structure and nearly the same interatomic spacings, growth may be achieved from a melt (solid A in contact with molten semiconductor B), from a vapor (solid A in contact with vapor containing constituent B in some form), or by evaporation (constituent B evaporated onto solid A). These processes of epitaxial growth are known respectively as *liquid-phase* epitaxy (LPE), *vapor-phase* epitaxy (VPE), and, when used to form compounds, the evaporative process is called *molecular-beam* epitaxy (MBE). VPE is a special case of *chemical vapor deposition* (CVD), which is employed to deposit an amorphous or polycrystalline layer on a substrate.

In order for the atoms arriving at the surface to lodge permanently at the proper sites—those associated with minimum energy—the atoms must be able to move to those sites over the surface of the solid. One can represent the energy of an atom on the surface of a one-dimensional solid by a sequence of regularly spaced hills and valleys (Fig. 9.3). Heating the solid can provide atoms on the surface with enough energy to surmount the barriers and move over the surface to the lower energy sites. It is even possible to heat a disordered solid layer on a dissimilar or similar crystalline solid substrate so as to produce an ordered crystalline layer (*solid-phase* epitaxy, SPE).

Single-Crystal Growth by Czochralski, Float-Zone, and Bridgman Techniques

To form single-crystal silicon ingots, either the Czochralski (CZ) or the float-zone (FZ) solidification process is employed. In the CZ process, a small oriented piece of single-crystal silicon used as a seed is put into contact with the surface of the molten silicon in a crucible that is rotated slowly. Silicon

from the melt freezes on the seed, which is slowly raised, resulting in the formation of a cylindrical single-crystal ingot from 7.5 to 12.5 cm in diameter and up to a meter long. Some purification also occurs during CZ growth, as can be seen from the phase diagram of Fig. 9.4. If constituent B is silicon and A is an impurity, the first solid to freeze will contain much less of impurity A than does the melt in contact with the solid that is forming.

In the float-zone method, a molten zone is passed through a relatively pure silicon ingot, causing a redistribution of impurities much as in the case of CZ growth. Because impurity concentrations are generally higher in the liquid, passage of thin molten zones through an ingot having a 0.01 percent impurity content causes impurities to be swept to one end of the ingot, leaving in the middle a region having an impurity content as small as one part in 10^{10}. Finally, the cylindrical ingot is cut with saws into round wafers about 250 μm thick.

Another important single-crystal growth technique is the Bridgman process, in which an oriented seed crystal is located at one end of a crucible containing the liquid, relatively pure semiconductor. Solidification occurs as the crucible or boat passes slowly through a region where the temperature is lowered to a value below the freezing temperature of the solid. This method (or CZ growth) is typically used for the growth and partial purification of GaAs. In growing GaAs by the Bridgman process one may start with liquid Ga in a sealed chamber that also contains a source of As. At the growth temperature, which is near the melting point of GaAs, 1240°C, the As source produces a vapor of As atoms at one atmosphere pressure, and stoichiometry of the GaAs results.

Growth must be relatively slow if single crystals are to result. The growth

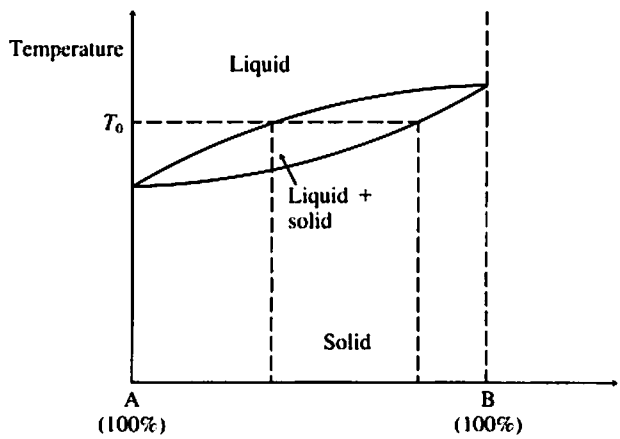


Figure 9.4 Hypothetical phase diagram for a two-component system. The constituents are labeled *A* and *B*.

rates for the CZ, FZ, and Bridgman techniques are typically on the order of centimeters per hour.

Polycrystalline Cells

The trade-offs of simpler and faster fabrication methods are well illustrated by the important example of polycrystalline solar cells. Polycrystalline silicon cells are made from square wafers of polycrystalline silicon cut from a solid that cooled from a melt. The grains in these cells have diameters of up to several millimeters, but the cells are otherwise similar to single crystal *pn*-junction Si cells. They have a diffused or implanted front layer, a metal front contact grid and a solid back electrode. Their square shape enables one to fill an array completely with these cells rather than leaving inactive areas as when one uses circular cells. Efficiencies up to 17 percent have been achieved (Storti, 1981). To correct for the loss of some carriers due to recombination at the grain boundaries, it has been possible to diffuse impurities along grain boundaries and thence a small distance into the individual grains to make the boundary regions serve to collect photo-generated current. This approach is shown in Fig. 9.5.

Improved Silicon Purification

The impact of improved processing in a particularly energy-intensive step in cell fabrication can be seen from two examples of ways of obtaining purer metallurgical grade silicon.

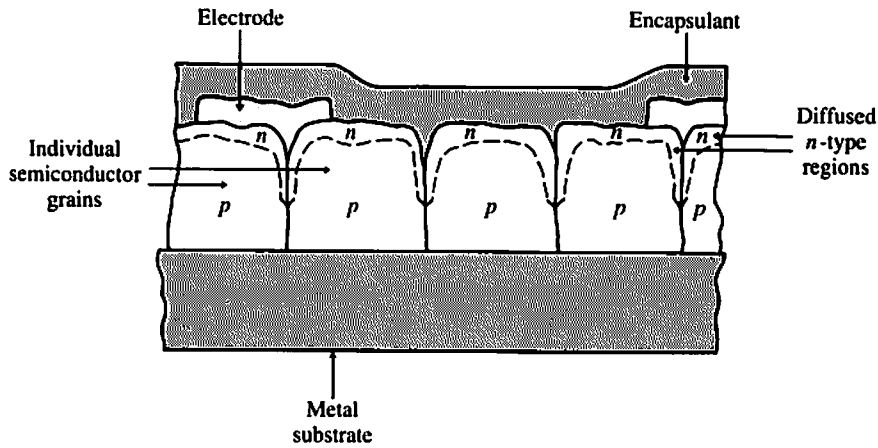


Figure 9.5 Cross-section of polycrystalline cell having diffused *n*-type regions partially surrounding each grain to collect carriers.

In Sec. 4.2.1 we showed that much of the energy payback time of conventional Si cell manufacture accrues in the silicon-refinement stage. It is possible to reduce the energy required there by using purer starting materials—naturally occurring quartzite pebbles having 99.5 percent SiO_2 content and refined charcoal that has been exposed to a halogen gas at high temperature for several hours (Lindmayer et al., 1977). When the molten silicon is cooled, unidirectional solidification can be employed and so some purification occurs then because of the segregation of impurities in the melt. If a polycrystalline starting material is acceptable for cell manufacture, a Czochralski process with a high pull rate can be used, resulting in further energy savings. The estimated cumulative payback time for this purification/refinement process is only 0.43 yr instead of the 2.84 yr cited earlier for the conventional reduction, refinement, and crystal-growth processes (these times do not include the energy expended in other steps in the cell fabrication process).

The energy payback time for these three processes can be lowered further to an estimated 0.18 years with a silicon fluoride polymer transport purification process (Lindmayer et al., 1977). Metallurgical-grade Si is exposed (at 1100°C) to SiF_4, producing gaseous SiF_2, which is then polymerized by chilling (to −45°C). Subsequent heating (to 400°C) produces amorphous Si and gaseous silicon fluorides, which escape and are recycled. Additional heating above 730°C causes the Si to crystallize and drives off all remaining silicon fluorides. Purification occurs at each stage of this process, making it quite economical in terms of the energy expended.

9.2 FORMING THIN SELF-SUPPORTING SEMICONDUCTOR RIBBONS AND SHEETS

Ingenious techniques exist for producing semiconductor plates thin enough to be made directly into solar cells without wafering. The desired thickness for silicon is from 0.1 to 0.3 mm. Single-crystal material is preferred for highest efficiency, although polycrystalline material is usable, particularly if the grains are large and their boundaries are mostly oriented parallel to the current-flow direction, perpendicular to the plane of the sheet. Furthermore, means are being developed for converting polycrystalline ribbons to single-crystal form, and for enlarging grains substantially in polycrystalline ribbons or sheets. One may also form a thin semiconducting sheet on a temporary substrate such as graphite or molybdenum and then remove the sheet for use in a cell. A dramatic new example of the use of the temporary substrate is the *rapid quenching process*—quenching at rates of up to a million degrees per second—originally used to form amorphous metal alloys (Chaudhari et al., 1980). Here molten silicon is sprayed onto a rapidly rotating, cooled metal

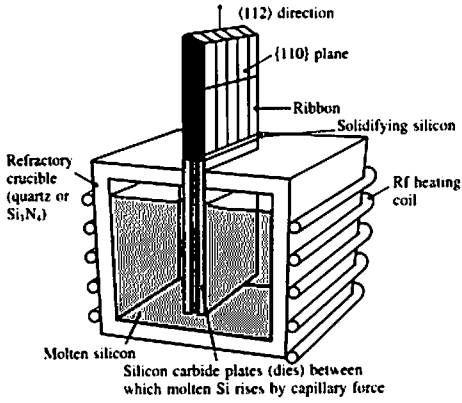
cylinder, where it crystallizes immediately to form a ribbon that moves tangentially away from the cylinder at high speed.

Low cost and large-scale utilization of solar cells demand high growth rates from any candidate processes, along with reasonable cell efficiencies. These are somewhat contradictory requirements since fast growth often results in imperfect crystals having numerous defects at which recombination can occur. Another problem is controlling contamination. If molten or very hot solid silicon is shaped by dies or rollers, reaction with those parts can produce both serious contamination of the semiconductor and deterioration of the apparatus. With silicon formed by condensation of a vapor at a solid surface, avoiding contamination may require the use of diffusion-barrier layers of metals having small diffusion coefficients for impurities present in the substrates.

Characteristics of some of the most promising of the ribbon and sheet processes are illustrated in Fig. 9.6 and summarized in Table 9.1. These are the *edge-defined film-fed* (EFG) ribbon and the *dendritic web* growth processes, the high-speed *rapid quenching* process, and several other processes where silicon is formed on a temporary substrate. The *ribbon-to-ribbon* (RTR) regrowth process employing laser heating enlarges the grains in polycrystalline material (see Sec. 9.4). Other interesting variations that have been suggested include forming doped silicon filaments from which one can weave a "cloth" having photovoltaic response, forming silicon layers on a glass substrate using the intermediary of an aluminum-silicon eutectic to avoid melting of the glass, and making tiny single-crystal doped silicon microspheres for use in a photoelectrochemical solar cell (described in Chap. 12).

The *edge-defined film-fed growth* process for silicon-ribbon growth (Ravi et al., 1975) was developed by Mobil-Tyco from its original use in growing sapphire tubes for high-pressure lamps. It involves pulling one or more Si ribbons 150 to 300 μm thick and up to 5 to 10 cm wide through a die mounted on a chamber containing molten Si (Fig. 9.6*a*). Growth in a desired direction is begun by the use of a seed first put into contact with the silicon melt. Interestingly, such thin silicon is flexible enough to be rolled like movie film onto a reel. Pull rates of 5 cm/min have been achieved and solar cell panels

Figure 9.6 Methods for producing self-supporting silicon ribbons and sheets: (*a*) Edge-defined film-fed growth (EFG) process. Multiple ribbons can be pulled from an apparatus having many dies and a single reservoir of molten silicon. (*b*) Stepanov ribbon process. (*c*) Dendritic web growth process for making Si ribbons up to 5 cm wide. [(*a*), (*b*), *and* (*c*) *from U.S. Patent 4,121,965.*] (*d*) Pulling broad Si sheet horizontally from the surface of a melt (schematic). (*e*) Schematic illustration of high-velocity rapid-quenching process, in which Si ribbon emerges at speeds up to tens of meters per second.


⟨112⟩ direction
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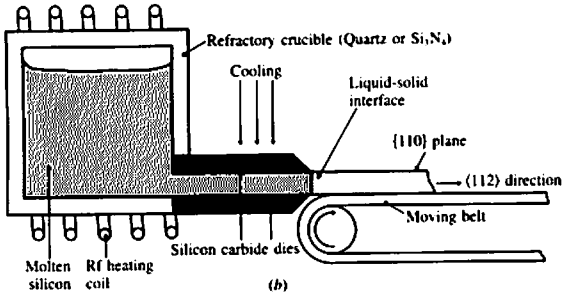
Ribbon
Solidifying silicon
Refractory crucible (quartz or Si_3N_4)
Rf heating coil
Molten silicon
Silicon carbide plates (dies) between which molten Si rises by capillary force

(a)


Refractory crucible (Quartz or Si_3N_4)
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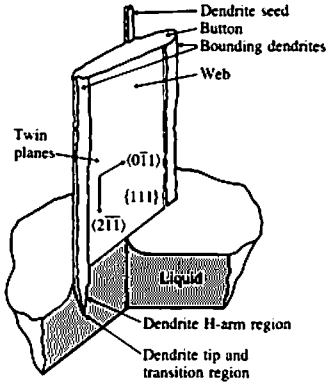
Molten silicon
Rf heating coil
Silicon carbide dies

(b)


Dendrite seed
Button
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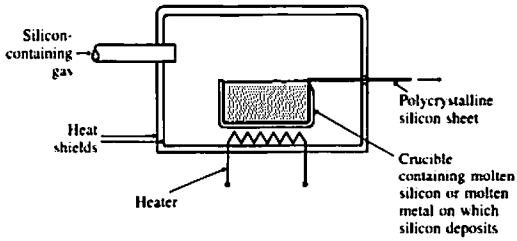
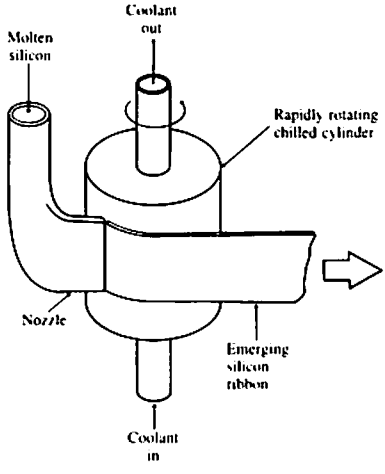
Dendrite tip and transition region

(c)


Silicon-containing gas
Heat shields
Heater
Polycrystalline silicon sheet
Crucible containing molten silicon or molten metal on which silicon deposits

(d)


Molten silicon
Coolant out
Rapidly rotating chilled cylinder
Nozzle
Emerging silicon ribbon
Coolant in

(e)

Table 9.1 Characteristics of some rapid silicon-growth techniques
Where two values are given, upper ones are best reported values and lower are typical results

Process	Experimental cell efficiency, %	Growth rate, cm/min	Width, cm	Thickness, μm	Continuous growth results
EFG ribbon	13–14 10–11	5 2.5–4	5–10	150–200 250–300	five 30-m lengths, 15 hrs
Dendritic web	15.5 12–13	7 3–4	4.7 3.5–4	50 150	3- to 4-m lengths, 17 hrs
Horizontal ribbon growth	9–10	41.5	5 1–3	200–350 400–2000	Greater than 5-m length
Low-angle silicon sheet	?	20–60	0.8–2.5	300–1000	0.75-m length
Rapid-quenching ribbon	5–8	1.8×10^5 (30 m/s)	0.1–1 (to 5 with double roller)	20–200	
Ribbon-to-ribbon regrowth	13 11–12	9 2.5–5	7.5 3.5	100 150–200	30-cm lengths
Silicon-on-ceramic	10.1 9	15 4–5	10 5	100 200	50-cm lengths

Source: Surek, 1980; Arai, 1980.

having 11 percent overall efficiency have been made from EFG ribbon. The economics of using such ribbon in an automated continuous solar cell factory are summarized in Sec. 9.6. Chief technical difficulties are the dissolving of the SiC die in the highly reactive molten Si, and the formation of crystal twins in the ribbon, which increases recombination at the boundaries. In the closely related *Stepanov process* (Fig. 9.6*b*), silicon is pulled horizontally from a hole formed by a die in the bottom of a heated boat, again resulting in essentially single-crystal ribbon having final thickness (Leipold, 1978).

Process parameters and characteristics of cells made from EFG material are listed in Table 9.1, along with those of the other ribbon, sheet, and layer processes described in this chapter. No clearly "best" process is yet evident since none of the processes receives consistently high marks in all the important characteristics required for high-quantity production of cells producing low-cost electricity.

In the *dendritic web* process (Fig. 9.6*c*), no die is used. A thin Si web is grown between two dendrites formed by pulling on a suitable seed initially in contact with a pool of molten Si. Growth rates up to 7 cm/min are obtained. Close control of temperatures and pulling rate is required, and the web surface is quite smooth. The advantages of the dendritic web process can be obtained with less difficult thermal control by growing a web between two graphite or quartz filaments pulled through a silicon melt (*edge-supported* pulling process) (Ciszek and Hurd, 1980). Both the dendritic web and the EFG processes have been put into at least pilot production, and in 1980 a formal arrangement was announced between a web manufacturer, Westinghouse, and two large electric power companies to begin production and evaluation on a commercial scale.

Horizontal ribbon growth by pulling a sheet horizontally from the surface of a melt permits somewhat higher rates of production than provided by the preceding ribbon techniques (Fig. 9.6*d*). This is because the large surface-to-volume ratio of the silicon permits more rapid removal of heat by radiation and convection from the emerging sheet. This process should have fewer problems associated with dissolving of the die than does the EFG process.

A very high rate of ribbon production is achieved by the *rapid quenching* process (Fig. 9.6*e*). Molten Si at 1500°C is ejected in air from a quartz tube onto a chilled copper cylinder 40 cm in diameter spinning at 100 r/min (Arai et al., 1980). The Si quenches as a polycrystalline ribbon with 20- to 30-μm diameter columnar grains whose axes are perpendicular to the ribbon plane. Doping to form a surface layer of different conductivity type can be accomplished, it is claimed, by ejecting an impurity-containing vapor onto the emerging ribbon downstream from where it leaves the cylinder. Ribbon widths from 1 to 50 mm, thicknesses from 20 to 200 μm, and linear velocities from 10 to 40 m/s are said to be possible. With a 20-m/s ribbon velocity—45 mi/h—one quenching apparatus could form 3 km^2 of 50-mm-wide ribbon in a year, corresponding to an impressive 300-MW_{pk} output in AM1 sunlight if

the cell efficiency were 10 percent. In early experiments 5 percent efficient cells were obtained, not by the vapor-doping method but by use of an n-type Si layer produced by chemical vapor deposition (CVD) on the p-type ribbons.

Another method for producing self-supporting polycrystalline ribbons is removing molten Si from the bottom of a heated container by squeezing it to the desired thickness between chilled rollers. Other workers have examined the feasibility of forming thin sheets by solidification on a temporary substrate such as a molybdenum sheet, in the case of both Si and GaAs. In one such process, the difference in thermal expansion coefficients of the 100- to 250-μm thick Si film and the Mo substrate causes the Si film to peel off upon cooling; after grain growth induced by the RTR process (Sec. 9.4), cells were made having AM1 efficiencies as high as 11.8 percent (Sarma and Rice, 1980). A process involving the cleavage of lateral epitaxial films for transfer to another substrate (the CLEFT process) is described in the next section, where formation of films on substrates is considered.

9.3 FORMING A SEMICONDUCTOR LAYER ON A SUBSTRATE

Single-crystal semiconductor layers grown slowly, under near thermal-equilibrium conditions, on a regular oriented solid substrate, may have excellent electrical and optical properties. Such layers may be used as the body of the solar cell, as a front-contact layer of opposite conductivity type, or as a layer for surface passivation and optical transmission as in the case of the GaAlAs layer on a crystalline GaAs cell.

Traditional processes for forming single-crystal layers by epitaxy—growth upon an oriented substrate—by the LPE or VPE processes have involved naturally occurring single-crystal substrates. Growth rates are typically between a micron per minute and a micron per hour, and growth temperatures range from hundreds to a thousand or more degrees centigrade. The change in properties at the interface is abrupt, and usually a fairly close match of lattice dimensions is required of the substrate and the layer, along with similarity of the thermal-expansion coefficients of those materials.

The molecular beam epitaxy (MBE) process is like VPE but with important differences. An ultra-high vacuum in the 10^{-10} Torr range is used for MBE, and evaporated atoms from heated sources form the growing layers, resulting in a fairly low growth rate on the order of tens of angstroms per minute. With MBE, semiconductors having compositions that cannot be achieved in thermal-equilibrium growth have been made, opening the possibility of tailoring electrical and optical properties, including the energy gap. Although applicable to solar cell work, it is doubtful that MBE will be

inexpensive enough to be used extensively for making nonconcentrator solar cells; the process may be useful for making small, high-efficiency multicolor concentrator cells, however.

Epitaxy on artificially regular surfaces formed by texturing photolithographically with a periodic pattern written with an electron beam has recently been achieved and christened "graphoepitaxy" (Geis et al., 1979). Single-crystal silicon has been formed by repeatedly laser-heating a 300-nm-thick amorphous silicon film grown by CVD on an amorphous silica substrate into which 100-nm-deep grooves having a 3.8-μm period were made by etching. It may be possible to mass-produce inexpensive textured surfaces for graphoepitaxy by embossing or injection-molding from a master, as is done with the videodisc—phonograph-recordlike disks having micron-sized depressions that store video information for later readout by a scanned low-power laser beam.

Very promising early results have been obtained with the so-called CLEFT process (McClelland et al., 1980), in which a thin semiconductor film is grown on and then cleaved from a substrate. CLEFT is an acronym for *c*leavage of *l*ateral *e*pitaxial *f*ilms for *t*ransfer. The method can be used with silicon, gallium arsenide, and probably other semiconductors. In one experiment, a carbonized photoresist mask having narrow, widely spaced stripe openings was formed on a (110) GaAs substrate that was placed in a VPE chamber. Epitaxial growth starts in the openings and then proceeds laterally over the mask, producing a continuous single-crystal GaAs film that can be cleaved from the reusable substrate. A 17 percent efficient GaAs single-junction cell has been made by the CLEFT process.

The many ways of depositing *polycrystalline semiconductor layers* that may be used for solar cells include the following:

- Evaporation from a boat of the semiconductor, possibly heated by an electron beam to maintain purity, onto an inexpensive inert substrate. An example is the evaporation of GaAs from a boat containing the compound onto graphite-coated molybdenum sheets.
- CVD-formed semiconductor layers on an inexpensive substrate. GaAs films 10 μm thick formed on tungsten-coated graphite have been used to make 8.5 percent efficient MOS cells (Chu et al., 1981).
- Columnar polycrystalline deposits having 10-μm-diameter grains of both Si and GaAs have been made by evaporation at rates up to 1 μm/min onto aluminum films, which form the back ohmic contact, on a glazed alumina ceramic support. An electron beam (E-gun) is used to heat the Si source ingot; in the GaAs deposition, the Ga source is heated with an electron beam while As is evaporated from a resistance-heated quartz crucible. Small grain size and contamination from the substrate remain problems.

- Evaporation onto thin flexible plastic substrates, such as mylar and kapton, of semiconductors such as CdS was demonstrated and used years ago in space cells that were unrolled in orbit, suggesting the possibility of making and installing terrestrial cells in a similar way.
- Polycrystalline deposits of elemental and compound semiconductors such as Ge, Si, and ZnO, as well as AR coatings, can be made by sputtering: in a chamber containing an ionized inert gas at low pressure, bombardment by the ions knocks atoms from a source (a plate or powder of semiconductor) so that they ultimately deposit on the desired substrate located in the chamber. Ionization may be produced by a dc or rf power supply. Deposition rates may exceed 20 μm/hr, and very large continuous-flow magnetron sputtering systems exist (for putting partially reflective coatings on sheets of window glass).
- "Silicon-on-ceramic" cells made from films of Si produced by dipping a substrate such as mullite ($3Al_2O_3 \cdot 3SiO_2$) into molten Si have been evaluated and found to yield up to 10.5 percent efficiency, as quoted by Feucht (1980).
- In the *ribbon-against-drop* process, a 300-μm-thick graphite ribbon coated with 5-μm-thick carbon deposited by pyrolysis is drawn at 7 cm/min through a close-fitting die in the bottom of a chamber of molten Si. The result is a coating of the ribbon by a polycrystalline Si layer less than 100 μm thick. The meniscus at the die prevents leakage from the chamber. Cells having 8 percent AM1 efficiency have been made this way.
- Manufacture of cadmium sulfide cells on glass emerging at the end of the production line of a float-glass plant has been reported by several groups; the processes include evaporation and spraying.
- Semiconductor films potentially useful for solar cells have been made by electrochemical deposition (electroplating) either from an aqueous or a nonaqueous electrolyte. These electrochemical processes are very efficient, can produce oriented granules, are fast with 1-μm/min and higher deposition rates for metals, and are suitable for large-scale, high-volume production. To date, reported efficiencies have been disappointingly low.
- A fascinating variant on these methods for producing uniform continuous coatings is the silicon shot process, described more fully in Chap. 12 in connection with photoelectrochemical cells. Tiny silicon spheres made like lead shot in a cooling tower are embedded in a plastic sheet and exposed to sunlight while in contact with a liquid electrolyte.

Amorphous semiconductor films have been produced in plasma discharge systems, for use in solar cells that are expected to be very inexpensive. Because its properties are quite different from those of either single-crystal or polycrystalline forms of the same semiconductor, amorphous material and means for its production will be discussed in Chap. 10, where unconventional solar cell materials are considered.

9.4 USE OF ION IMPLANTATION, LASERS, AND ELECTRON BEAMS

Doping semiconductors by ion implantation is a standard integrated-circuit-processing technique that is expected to be important in solar cell manufacture. Implanters operating with beam voltages from 10 to more than 300 keV are commercially available, permitting one to produce impurity densities up to about 10^{16} cm^{-2} in continous processing of Si wafers loaded in automatically handled cassettes. Throughputs of 250 to 300 4-in-diameter wafers per hour are possible, at costs around \$0.01 to 0.02/cm^2 (1980 dollars).

In addition to forming the front contact layer, ion implantation can be used to deposit a backside layer in back-surface-field (BSF) cells where minority carriers are deliberately reflected from the heavily doped back contact. Another potential use of implantation is in *gettering*, a process that can be used to increase minority-carrier lifetime in semiconductors by sweeping lifetime-killing impurities and certain crystal defects away from crucial regions of a semiconductor device. In gettering with impurities, a dopant is deposited to a high density by implantation (or by thermal diffusion) through the back surface of a cell. Typical dopants are P or Ar, at densitites around 5×10^{15} cm^{-2}. When the wafer is later heated in an inert atmosphere (for example, at 850°C in forming gas), interstitial impurity atoms and crystal defects migrate through the crystal and become trapped at the doped surface, where they may be removed with a chemical etchant or left where they do not affect device performance. An alternative gettering process involves simply damaging the back surface mechanically before heating. These processes are found to increase the lifetime markedly, and have been used commercially for recycling reject wafers from the IC industry.

Thermal energy is usually required for atoms in a solid to move about at an appreciable rate. In conventional semiconductor processing, heating occurs primarily by radiation from a resistive heater, held at constant temperature, surrounding a fused quartz furnace tube containing a high-purity gas. New methods of heating involving transient energy input to the semiconductor with intense light or high-density electron beams appear very attractive for solar cell manufacture.

Heating may be used for diffusing dopants, for healing the lattice damage caused by ion implantation, enabling grains of a polycrystalline solid to grow larger, relieving strains caused by unequal thermal expansion in a multilayer semiconductor structure, promoting chemical reactions such as oxidation and epitaxy, sintering surface layers, and even melting surface layers or particularly susceptible layers inside a solid. Using intense electron beams or light from a laser or an intense incoherent light source can be efficient—since the

energy can be deposited just where it is needed—and fast, permitting a high throughput.

Two different regimes of heating with electron beams and light are distinguished: a *pulsed* regime involving brief pulses of high-enough energy density to cause melting of part of the irradiated solid, and a *scanned* regime characterized by a more gradual deposition of energy that may or may not be sufficient to cause melting but is adequate for producing rapid diffusion of atoms in the solid. In the pulsed mode, electron beam or Q-switched laser peak intensities up to 10 MW/cm^2 are used, so that surface temperatures rise in a few microseconds from the steady substrate temperature to the melting temperature. When melting occurs, in a layer about a micron thick, atoms mix rapidly in the melt, causing the concentration profile of implanted dopants to change from gaussian or near-gaussian shape to a uniform distribution, as shown in Fig. 9.7. At lower intensities in the scanning mode, a continuous electron beam or ion laser beam is swept at a rate of a few centimeters per second, electronically or mechanically respectively, over the surface of the semiconductor mounted on a stage heated to an average temperature around 300°C. Atomic rearrangement can take place (solid-state epitaxial regrowth), although melting does not occur, to activate impurities—

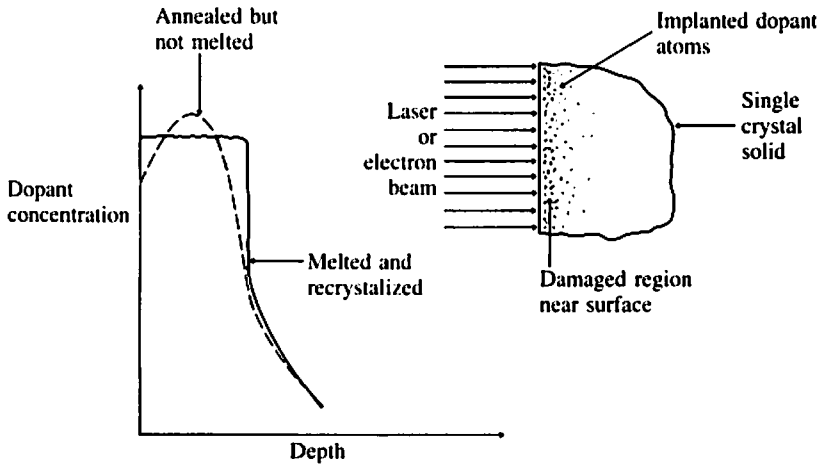


Figure 9.7 Dopant profiles obtained by ion implantation and laser- or electron-beam annealing. Inset shows distribution of atoms after implantation, with damaged surface layer and electrically inactive dopant atoms. Use of intense pulsed laser or electron-beam irradiation causes melting of the surface layer and uniform redistribution of dopants in the layer. Lower temperature heating also activates impurities and removes damage but does not redistribute the dopants, allowing the impurity profiles obtained by control of implant conditions to be retained.

allow them to move into substitutional sites where they ionize—and to heal lattice damage.

It has been shown that scanned electron beam and laser annealing of implants can activate implanted impurities as fully as does thermal annealing. The effects upon minority-carrier lifetime have not yet been clearly established. Electron beam systems convert primary power to beam power much more efficiently than do lasers, but require the semiconductor to be in a vacuum. Inclusion of a pulsed electron beam source or introduction of a laser beam through a window in an ion-implantation machine for annealing permits both processes to be done in a single pumpdown. With optical heating, the penetration depth can be controlled by the choice of wavelength, within practical limits based on available high-intensity light sources. The use of concentrated sunlight as a source is an intriguing but perhaps impractical idea, compatible with the "solar breeder" factory described in Sec. 9.6.

Recrystallization of ribbon by laser heating (the ribbon-to-ribbon, or RTR, process) is illustrated in Fig. 9.8. The growth of crystals having desired directions is promoted by heating, which permits atomic rearrangement but not actual melting, and a thinner, single-crystal ribbon emerges at the top of the recrystallization apparatus. Conversion of inexpensively deposited amor-

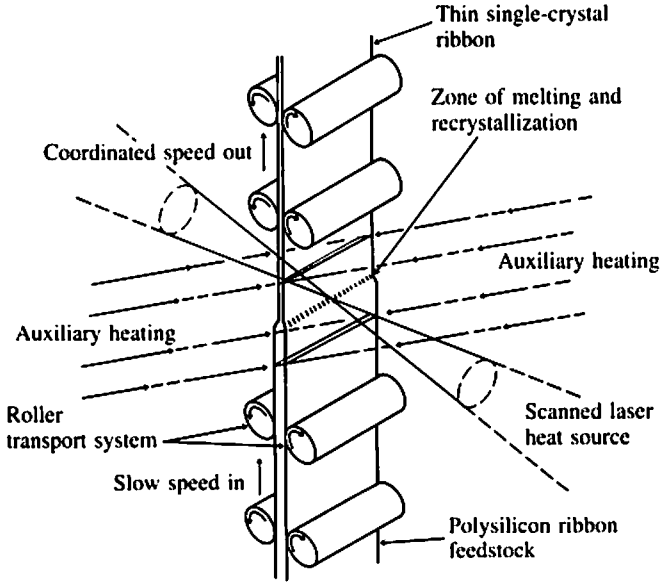


Figure 9.8 Ribbon-to-ribbon process for converting a polycrystalline silicon ribbon entering at bottom into thin, single-crystal ribbon by controlled laser heating. (*From Jet Propulsion Laboratory, California Institute of Technology, "Low Cost Solar Array Project Quarterly Report No. 9, April–June 1978," Pasadena, CA, 1979.*)

phous Si and GaAs into crystalline form has been demonstrated, as mentioned in Sec. 9.3, and as described in experiments with a graphite strip heater moved slowly laterally near the surface of an amorphous semiconductor (Tsaur et al., 1981). Successful grain enlargement and polycrystalline regrowth of Si and GaAs have been reported by many workers.

9.5 OPTICAL COATINGS, CONTACTS, AND ENCAPSULANTS

The topics of this section will be treated briefly since the aims of increasing production rate and lowering cost of optical coatings, contacts, and encapsulants appear to be attainable by fairly straightforward means. For example, presently most solar cell AR coatings are deposited on 20 or 30 wafers mounted together in an evacuated chamber by evaporation of oxides or fluorides from a heated filament or boat. For larger production rates, continous processing must be used, whether it be evaporation or magnetron sputtering, with cells moved automatically into and out of the coating chamber through air locks. Some alternative processes that might find use in optical coating are the use of sprayed or spun-on liquid coatings, in precisely controlled amounts, which are then fired to yield dense and durable coatings. Where glass sheets are used for encapsulation, chemical leaching of the surface is a fast way of removing material at the glass–air interface to make the change of index of refraction less abrupt and so increase optical transmission. Electrochemical means such as electroplating followed by anodic-oxidation (anodization) is a high-rate, low-cost process that has already been used experimentally to form AR coatings.

The dimensions of the solar cell electrodes are large, at least on nonconcentrator cells, compared with the dimensions now common in ICs, permitting the use of processes akin to printing—electrode "ink" consisting of metal powders mixed with an organic binder and perhaps very small beads of low-melting-point glass (frit) is printed or silk-screened on the semiconductor and then fired. In Schottky-barrier cells, the careful control of the thickness of the broad area electrode to permit both optical transmission and current collection likely will require use of evaporation or magnetron sputtering combined with feedback from an electrical or optical thickness-monitoring system. A heavily doped semiconductor having a wide bandgap can serve as a transparent conducting electrode in Schottky-barrier cells. The outstanding example is indium-tin oxide (ITO), discussed in Sec. 10.3.

Encapsulation with either glass or compliant rubbery substances has proved most reliable in solar cell tests to date, although it is claimed that suitable varnishes have been found that protect the cadmium sulfide cells made on a float-glass substrate. For example, in marine solar arrays polyvinyl

butyral has been used as a resilient encapsulant, and butyl rubber as an edge sealant. Glasses have been bonded electrostatically—by the field-assisted bonding process—to oxidized semiconductors and metals by applying briefly an electric field around 10 kV/cm to a sandwich consisting of glass in close contact with the semiconductor between electrodes (with the negative on the glass side) heated to several hundred degrees centigrade. It appears possible with some concentrator cell designs to encapsulate the cell almost entirely in glass, leaving open only the backside of the semiconductor for heat transfer. Solder glass frits which can be melted with intense infrared radiation may also be useful in encapsulating finished cells.

9.6 CONTINUOUS CELL PRODUCTION IN AN AUTOMATED FACTORY

Simulation with the SAMICS computer methodology for analyzing the manufacture of solar cells (see Appendix 7) has shown that an automated factory based on a silicon-ribbon technology can produce cells that meet the 1986 DOE cost goals—provided certain assumptions are valid.

A crucial assumption is that polycrystalline metallurgical-grade silicon (MG–Si) is available at \$14/kg (1980 dollars). In large quantities, such as the 1000 metric tons that would be required annually for the 250 MW/yr factory discussed below, silicon made conventionally costs about \$56/kg (1980 dollars). It is claimed that processes under development could result in prices ranging from \$10/kg to \$14/kg. The silicon cost is only one element in the overall array cost, so the estimated cost per watt for the processing described below to make 12 percent efficient arrays would only increase from \$0.63/W_{pk} with \$10/kg silicon to \$0.85/W_{pk} if one had to use the \$56/kg silicon available now (again, the 1986 DOE target is \$0.70/W_{pk}).

The business assumptions are based on a conventional capitalistic framework with amortization of equipment facilities, a 100 percent overhead rate on direct costs, 20 percent return on invested capital, 9.25 percent interest rate on borrowed capital, and a 1:6 debt-to-equity ratio. Ordinary corporate taxation and normal tax credits are assumed. The factory, having a 250-MW annual capacity, would operate round-the-clock and all of its product is assumed to be sold.

Silicon ribbon producing 12 percent efficient encapsulated AM1 panels is assumed. Five 7.5-cm-wide EFG ribbons are pulled from each furnace at 7.5 cm/min. Other ribbon technologies such as the dendritic web or the high-speed rapid-quenching process would also be usable, of course, at possibly lower cost.

The processing assumed follows, and the estimated costs appear in Table 9.2. A p^+ back contact is made by applying and firing-in aluminum powder

Table 9.2 Annual cost in $/$W_{pk}$ for process steps in hypothetical automated factory producing solar panels with continuous processes

Values in 1975 dollars. Encapsulated cells assumed 12% efficient; $10/kg silicon assumed

Process	% total value added	Value added	Capital costs	Direct labor	Materials and supplies	Utilities	Indirect expenses	Yield
Silicon preparation	~10	$0.043			$0.0434			
Sheet fabrication	~31	0.145	0.0630	0.0312	0.0140	0.0049	0.0320	0.800
Cell fabrication	~23							
p^+ Back		0.002	0.0010	0.0004	0.0002	0.0000	0.0005	0.998
Etch		0.010	0.0036	0.0018	0.0033	0.0000	0.0018	0.994
Ion implant		0.012	0.0067	0.0018	0.0000	0.0003	0.0032	0.998
Pulse anneal		0.006	0.0038	0.0004	0.0000	0.0003	0.0011	0.992
Back metallization		0.036	0.0108	0.0013	0.0206	0.0005	0.0030	0.980
Front metallization		0.036	0.0111	0.0013	0.0202	0.0005	0.0030	0.980
AR coating		0.009	0.0038	0.0018	0.0014	0.0002	0.0016	0.990
Interconnection, packaging, and testing	~36	0.033	0.0104	0.0040	0.0135	0.0000	0.0054	0.999
Interconnect								
Encapsulate and assemble		0.130	0.0368	0.0062	0.0750	0.0001	0.0120	0.999
Test		0.001	0.0003	0.0002	0.0000	0.0000	0.0002	0.980
Package		0.001	0.0002	0.0001	0.0002	0.0000	0.0001	0.9999
Total	100%	$0.464	0.1515	0.0505	$0.1918	0.0068	0.0639	—

Source: Aster, 1978.

on the back of the wafer. Before ion implantation and pulsed annealing of the front layer of the junction, a plasma etch removes the thin oxide that forms naturally on the wafer. Screen-printed silver paste forms the back and front contacts, and a sprayed antireflection coating is applied. Cells are interconnected into 1.2-m-long strings of 12 cells each, and then 16 such strings (192 cells) are connected into a 4-ft^2 module, and encapsulated between a 3-mm-thick float glass and a 0.005-in-thick mylar back layer, with ethylene vinyl acetate sheets between. There is an edge seal and an aluminum frame. Incidentally, the encapsulation materials, excepting cells and interconnects, would cost around \$12/m^2 (1980 dollars). Modules are then tested and packaged. Moving belts would transport parts from one work station to the next for high throughput and low labor cost. Throughput at some stations would exceed 60 cells per minute, and the total processing time from semiconductor stock to module could be as short as two hours. Of the processes listed, cost estimates for the pulse annealing of the ion implant are not firm because this process, though shown to work, is not operated today on a commercial scale. Printing of electrodes and contacts also may require some further development for large-scale use.

Note that in Table 9.2 the estimated silicon cost is only about 10 percent of the final cost, and that sheet fabrication and final assembly of cells into encapsulated modules each account for about one third of the total added value. The sheet fabrication is the most expensive item in terms of both capital and labor requirements per watt of cell output; the encapsulation and assembly involve the highest material and supply costs. Energy payback times for the steps shown are estimated at about two months for the 12 percent cells, *excluding* the energy for constructing the factory and energy for silicon production. The amount of silicon used is only about a third of that required by an advanced ingot technology, causing a corresponding reduction of the estimated energy payback time down to slightly less than one year.

Solar Breeder Plant

One intriguing concept is a solar cell plant whose only direct energy input is sunlight incident on arrays of solar cells on its roof (Lindmayer et al., 1977)—the "solar breeder," a logical alternative to the nuclear version. Perhaps simply on principle, direct solar thermal input has been avoided in the design, although it could also be used. To handle the problem of intermittency of sunshine, two forms of storage are envisioned—electrical storage in batteries, and temporary storage of partially completed objects between manufacturing stations. Equipment such as large furnaces in the plant must be operated continuously, but other equipment could be run intermittently as energy supply and demand for particular parts fluctuate. Computer control of processing, now common in IC manufacture, will be particularly important

in this case because of the need for responding appropriately to the fluctuating energy input.

9.7 SUMMARY

Process heat employed in making conventional solar cells contributes significantly to cell cost. Improved processing techniques aimed at achieving low costs involve reducing the heat required—through improved refinement and purification processing, and utilizing polycrystalline semiconductors. By using thin sheets of semiconductor formed directly rather than by sawing from an ingot, one can realize additional important savings of material, energy, and labor. Examples of the latter are the dendritic-web silicon-growth process, and the CLEFT process for growing single-crystal Si or GaAs sheets that are later separated mechanically from their growth substrates.

Recrystallization of rapidly grown polycrystalline layers should raise the efficiencies of the cells, and automated large-volume cell manufacturing and array assembly should help make solar cells competitive with conventional power sources.

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PROBLEMS

9.1 *Thermal activation and impurity diffusion* The atomic diffusion constant D at any absolute temperature T for a given impurity in silicon can be written as $D = D_0 e^{-E_a/kT}$, where E_a is an activation energy, k is the Boltzmann constant, and D_0 is a constant that depends on the type of impurity. In a time t atoms will diffuse a mean distance $L = 2(Dt)^{1/2}$, where L is known as the atomic diffusion length. From the data below, determine how long it would take at 100°C for boron (used intentionally as a dopant) and copper (an unwanted contaminant) to diffuse entirely through a 100-μm-thick silicon solar cell, making it inoperable.

Impurity atom	Temperature, T	D, $\mu m^2/h$
Boron	1573 K (1300°C)	2.9
	1173 K (900°C)	3.2×10^{-4}
Copper	1573 K (1300°C)	6.4×10^{7}
	1173 K (900°C)	1.9×10^{7}

9.2 *Production rates, improved processes* Referring back to the example of Chap. 4 for meeting 10 percent of the U.S. electricity demand in the year 2000 with PV systems, calculate the number of EFG ribbon or dendritic web machines required to meet the annual production rate. Assume the best of the characteristics of these processes listed in Table 9.1. Compare with the value for the rapid-quenching process.

9.3 *Nonthermal processing methods* The nonthermal processes described in this chapter that use ion implantation, lasers, or electron beams tend to be more energy efficient than entirely thermal processes, such as CZ growth and thermal diffusion. Identify where input energy is lost in these different processes (i.e., fails to produce a useful result). What constraints on the wavelengths used in laser regrowth (Fig. 9.8) can you identify?

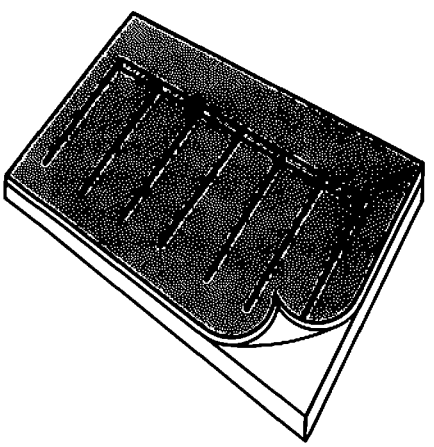
9.4 *Solar cell factory* Describe your visions for the most advanced silicon solar cell manufacturing plants that will be operational in 10 yr and in 20 yr. Be specific. You may also describe the raw materials and the finished products.

CHAPTER

TEN

THIN-FILM AND UNCONVENTIONAL CELL MATERIALS

CHAPTER OUTLINE



Of the many substances that exhibit the photovoltaic effect, cells having AM1 efficiencies greater than 15 percent have been made with only two materials—Si and GaAs. On the other hand, cells with AM1 efficiencies greater than 5 percent have been made utilizing more than a dozen different semiconductors, and one may well wonder whether there is one "best" semiconductor material for solar cells.

The problem is that the promise or potential of a given material for PV use is not determined solely by the *intrinsic* properties of the semiconductor, and so no simple figure of merit for PV use exists. Important factors affecting cell behavior and cost, though hard to quantify, include cell structure (*pn* junction or MIS, for example), form in which the material is used (such as single-crystal or polycrystalline), the effects of processing upon carrier lifetime, suitability for large-scale manufacture, stability under changing ambient conditions, and material availability and potential toxicity. As a result, many different materials have been and are being investigated.

10.1 INTRODUCTION

The most important physical characteristic of a candidate solar cell semiconductor is the energy gap, since it determines to what fraction of the solar spectrum the semiconductor can respond. The maximum theoretical con-

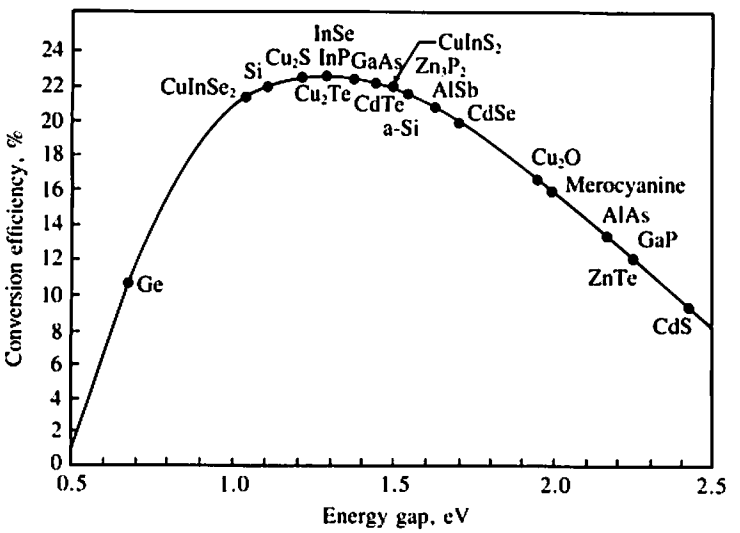


Figure 10.1 Maximum theoretical conversion efficiency vs. energy gap for solar cells in AM1 sunlight. Crystalline silicon is denoted Si, and amorphous silicon is a-Si. [*Barnett and Rothwarf (1980), as adapted from Prince (1955).* © *1980 IEEE.*]

version efficiency is plotted in Fig. 10.1 versus semiconductor energy gap. A number of semiconductors of current interest for solar cell applications are identified in the figure. Of great importance also is the optical absorption coefficient and its dependence upon photon energy, plotted in Fig. 10.2 for many semiconductors being considered for use in thin-film nonconcentrator cells. The AM1.5 solar spectrum is also shown in Fig. 10.2; semiconductors having an energy gap less than 1.7 eV would permit utilization of a significant portion of that spectrum. See also Fig. 3.5.

The qualitative effects of many of the characteristics or properties of semiconductors are listed in Table 10.1, which applies mostly to *pn*-junction cells. A more restricted list of the properties of many semiconductors appears in Table 10.2 where only energy gap and selected electrical properties appear. Of the commercially available cells discussed in Chap. 4, Si is the most used, even though its energy gap is not optimal, because the material is relatively inexpensive and the technology of processing it is well developed.

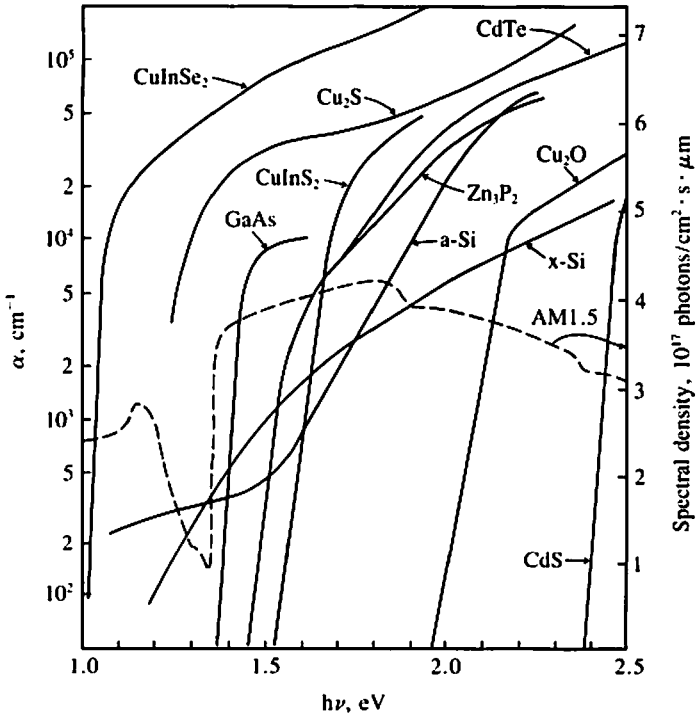


Figure 10.2 Optical absorption coefficient vs. photon energy for various semiconductors. Crystalline and amorphous silicon are denoted x–Si and a–Si, respectively here. (*Barnett and Rothwarf, 1980. © 1980 IEEE.*)

Table 10.1 Semiconductor properties and their effects upon solar cell characteristics

Property	Characteristics affected
	Electrical
Size of energy gap	Portion of spectrum that is effective; V_{oc}; temperature sensitivity
Type of energy gap	Cell thickness (thickness needed is smaller if gap is direct); collection efficiency for given diffusion length
Minority-carrier lifetime	Percentage of photo-generated carriers collected; hence, J_{sc} and cell efficiency
Diffusion length	Collection efficiency; minimum allowable grain size
Conductivity types possible	Whether homojunction cell is possible
Mobility	Collection efficiency; series resistance
Possible conductivity	I^2R losses in thin front layers; junction width
Schottky-barrier height	V_{oc} and cell efficiency
Electron affinity	Shape of band diagram at Schottky and hetero-junctions; collection efficiency and V_{oc}
Contact resistance	I^2R loss
	Optical
Absorption coefficient	Cell thickness and material required
Index of refraction	AR coating required
	Thermal
Thermal conductivity	Ease of cooling concentrator cell
Expansion coefficient	Epitaxy possible? Compatibility with electrical contacts and encapsulants; heat transfer
	Other physical and chemical
Surface properties	Carrier lifetime; ability to passivate surface
Crystal class and orientation	Chemical etching characteristics for cell manufacture and texturing; ion implantation and annealing characteristics
Lattice constant	Epitaxy possible?
Impurity diffusion along grain boundaries	Polycrystalline and cell processing feasibility owing to carrier-lifetime reduction
Chemical stability	Useful life of cell; vulnerability of cell to attack by atmosphere
Physical stability	Useful life of cell; ability to stand high-temperature processing during manufacture; possible phase changes at moderate temperatures after manufacture

Table 10.2 Properties of semiconductors*

Group(s)	Semiconductor	Energy gap at 300 K, eV	Type of gap—direct or indirect	Refractive index, n	Mobility $cm^2/V \cdot s$		Reference
					Electron	Hole	
			Elements				
IV	Si	1.12	ind	3.44	1350	480	1
IV	Ge	0.67	ind	4.00	3900	1900	1
VI	Se	1.74	dir	5.56 c 3.72 c			1
VI	Te	0.32	dir	3.07 c 2.68 c	1100		1
			Binary compounds				
IV-IV	SiC (α)	2.8–3.2	ind				1
	SiC (β)	2.2	ind				1
III-V	BP	2	ind	2.6			1
III-V	AlP	2.43	ind	3.0	80		1
III-V	AlAs	2.16	ind		1000	~100	1
III-V	AlSb	1.6	ind	3.4	50	400	1
III-V	GaN	3.5	dir	2.4	150		
III-V	GaP	2.25	ind	3.37	120	120	1
III-V	GaAs	1.43	dir	3.4	8600	400	1
III-V	GaSb	0.69	dir	3.9	4000	650	1
III-V	InP	1.28	dir	3.37	4000	650	1
III-V	InAs	0.36	dir	3.42	30,000	240	1
III-V	InSb	0.17	dir	3.75	76,000	5000 (78 K)	1

II-VI	ZnO	3.2	dir	2.2	180		1
II-VI	ZnS (α)	3.8	dir	2.4			1
	ZnS (β)	3.6	dir	2.4			1
II-VI	ZnSe	2.58	dir	2.89	100		1
II-VI	ZnTe	2.28	dir	3.56			
II-VI	CdS	2.53	dir	2.5	210		1
II-VI	CdSe	1.74	dir		500		1
II-VI	CdTe	1.50	dir	2.75	600		1
II-VI	HgS	2.5	dir				
II-VI	HgSe	−0.15	dir		5500		1
II-VI	HgTe	−0.15	dir	3.7	2200		1
II-VI	InSe	1.3					2
IV-VI	PbS	0.37	dir	3.7	550	600	1
IV-VI	PbSe	0.26	dir		1020	930	1
IV-VI	PbTe	0.29	dir	3.8	1620	750	1
IV-VI	SnTe	0.18	dir				1
II-V	Zn_3P_2	1.5	dir				2
I-VI	Cu_2S	1.2	dir				2
I-VI	Cu_2Te	1.4					2
I-VI	Cu_2O	2	dir				2
			Ternary compounds				
I-III-VI	$CuInSe_2$	1.04	dir		320	10	2,3
I-III-VI	$CuInS_2$	1.55	dir		200	15	2,3
I-III-VI	$CuInTe_2$	0.96	dir		200	20	3
I-III-VI	$CuGaSe_2$	1.68	dir			20	3

*Data from the following sources: (1) Pankove (1971); (2) Barnett and Rothwarf (1980); (3) Chen and Mickelsen (1980). Note that estimates of index of refraction for a semiconductor of known energy gap can be obtained from the empirical rule $n^4E_g = 77$, obeyed by semiconductors for which n^4 lies between 30 and 440.

Recently, Barnett and Rothwarf (1980) have published a unified analysis of thin-film cells, which lays out an orderly procedure for evaluating cell materials. That work will be summarized in Sec. 10.4, following discussion of amorphous semiconductors (Sec. 10.2), and miscellaneous cell materials (Sec. 10.3).

10.2 AMORPHOUS SEMICONDUCTORS

The properties of a given semiconductor, such as silicon, when it is prepared in an amorphous state, differ markedly from those of the same material in crystalline form. The energy gap and optical absorption coefficient for amorphous silicon (a–Si) are both larger than for crystalline silicon, as shown in Figs. 10.1 and 10.2, and one can readily change these properties by altering the conditions under which the materials are prepared. Thus, very thin amorphous silicon films only about 1 μm thick can be used, and one can consider economical cell designs where film properties are graded through the thickness of the semiconductor for higher efficiency.

Early a–Si films made by vacuum evaporation or sputtering in an inert gas had such high concentrations of states in the energy gap resulting from defects that the films were considered useless for solar cell application. Startling improvement occurred when up to 35 atomic percent hydrogen was incorporated in the material, forming what has been termed an *amorphous silicon-hydrogen alloy,* a–Si:H. Such a material can be prepared simply by the decomposition of silane (SiH_4) in a glow discharge, or by sputtering in a hydrogen-containing atmosphere. The hydrogen atoms bond with the unpaired electrons on Si atoms whose outermost shells of valence electrons are incomplete: in a–Si every atom does not have four nearest Si neighbors, as in crystalline silicon. With these defect states removed by the hydrogen bonding, the electrical conductivity of a–Si:H drops dramatically—a 6 atomic percent hydrogen content causes conductivity to drop by a factor of 10^7 from that of pure a–Si.Thus a–Si:H can be doped n- and p-type by the addition of atoms of phosphorus and boron, for example, by admitting phosphine (PH_3) or diborane (B_2H_6) to the glow discharge chamber along with the silane (Spear et al., 1976). Further reduction of defect state density near the Fermi level results if the active element fluorine is also present, for example by depositing from a glow discharge in SiF_4H_2, producing an amorphous alloy of silicon, fluorine, and hydrogen (a–Si:F:H).

Desirable properties of these materials are the bandgap, which is adjustable from 1.5 to 2.9 eV, the high optical absorption coefficient (Fig. 10.3), and the demonstrated ability to form n or p-type material by doping. On the other hand, free carrier diffusion lengths in the early a-Si:H were very short,

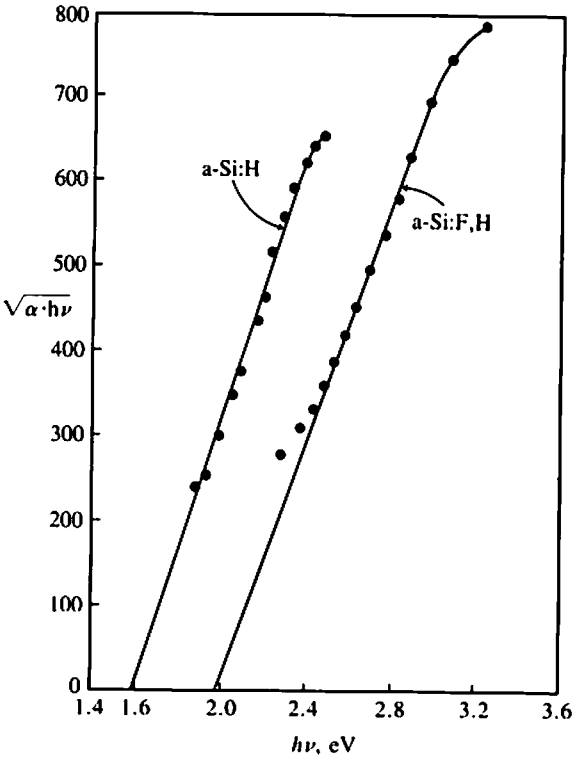


Figure 10.3 Optical absorption of amorphous silicon alloys vs. photon energy (vertical axis is square root of product of optical absorption coefficient and photon energy). (*Dalal, 1980. © 1980 IEEE.*)

typically less than 0.1 μm, which made collection of photo-generated carriers difficult.

The report from RCA of a small-area 5.5 percent efficient AM1 a-Si:H cell (Carlson, 1977) stimulated intense and continuing interest and activity. This cell was a metal-insulator-semiconductor (MIS) device employing a thin platinum electrode on the a-Si:H. Improved material and the use of *p-i-n* structure resulted in the significant achievement of single-junction amorphous silicon cells having AM1 efficiencies greater than 10 percent, a figure often taken as the lower limit for economically viable cells for power production (Catalano et al., 1982). This cell utilizes a wide bandgap *p*-type amorphous silicon carbide window layer on underlying a-Si:H intrinsic and *n*-type layers deposited on a reflective silver back contact. By increasing material purity and reducing defects in the intrinsic region, typical diffusion lengths there

were raised to 1 μm. Cell stability under illumination, a former problem, is said to be under control through attention to contamination during fabrication. Parameters for these 1.1-cm^2 experimental cells are: V_{oc} = 0.84 V, J_{sc} = 17.8 mA/cm^2, FF = 0.676, and η = 10.1 percent.

Amorphous Si cells already appear to have a place in consumer electronics, as mentioned in Chap. 7, because of their compatibility with integrated circuit fabrication techniques. The ease with which amorphous semiconductors having different energy gaps can be formed suggests that higher efficiencies may be achieved with multiple-gap amorphous cells. The multiple-gap cell, described more fully in Chap. 12, incorporates layers of semiconductors having different energy gaps; the light passes sequentially through layers having successively smaller gaps. Already an 8.5 percent efficient amorphous-silicon-based multiple-gap cell has been developed (Nakamura et al., 1982) consisting of three *p-i-n* structures on a supporting substrate. Light passes in turn through two different a-Si:H *p-i-n* cells and finally into an a-SiGe:H *p-i-n* cell having the smallest energy gap.

10.3 MISCELLANEOUS MATERIALS FOR SOLAR CELL USE

Several other materials deserve particular mention before we conclude this chapter with the discussion of thin-film cells (Sec. 10.4).

$CuInSe_2$/CdS Solar Cells

Through 1980, the only solar cells having AM1 efficiencies above 10 percent and employing semiconductors other than Si or GaAs involved epitaxial CdS, the single-crystal ternary compound $CuInSe_2$, or single-crystal InP on single-crystal CdS, discussed below. The 12 percent efficiency observed (Shay et al., 1975) with the single-crystal $CuInSe_2$/CdS has been followed by an impressive 9.4 percent AM1 efficiency in a one-square-centimeter area of polycrystalline thin-film $CuInSe_2$/CdS cell produced entirely by vacuum deposition and sputtering onto an inexpensive polycrystalline alumina substrate (Chen and Mickelsen, 1980).

Direct-gap (1.04 eV) *p*-type $CuInSe_2$ has a lattice constant that matches well with that of CdS, a condition favorable for epitaxy and minimizing recombination at the interface, as discussed below in Sec. 10.4. The heterojunction with n–CdS was made by successive evaporations in a single pump-down of a chamber containing Cu, In, Se, and CdS sources, onto a rf-sputtered molybdenum film on an alumina substrate. Following deposition of the selenide layers (see Fig. 10.4), which involved changing the substrate temperature in order to change resistivity, a shutter was opened to expose the

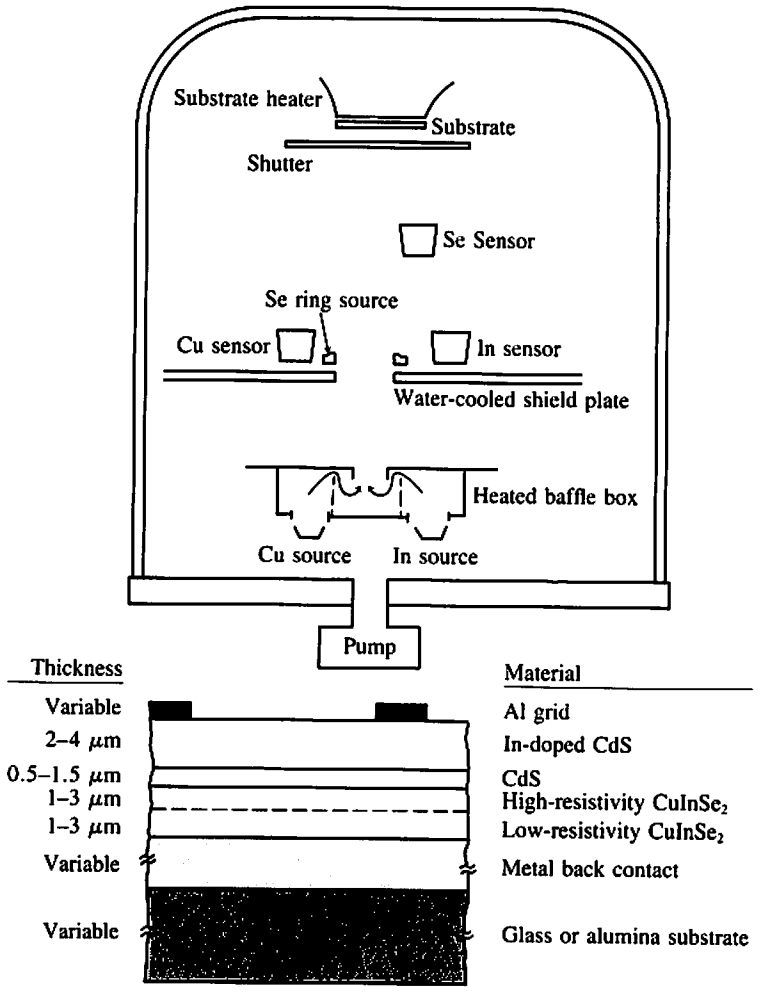


Figure 10.4 Schematic cross-section of 9.4 percent efficient AM1 $CuInSe_2/CdS$ heterojunction cell formed entirely by sputtering and evaporation, as shown at top. (*After Mickelsen and Chen, 1980.*)

tantalum CdS evaporation boat which had a conventional loose quartz wool plug to prevent spattering. Finally, an aluminum contact grid was evaporated through a metal mask.

InP Solar Cells

With a nearly ideal energy gap (1.4 eV), InP has a theoretical conversion efficiency near that of GaAs, and is a candidate for use particularly in thin-

film form (see Sec. 10.4). Recent achievement (Turner et al., 1980) of 15 percent AM1 efficiency in a *pn*-homojunction cell, formed by epitaxial growth of single-crystal *p*-type InP on a (100)-oriented p^+, Zn-doped InP single-crystal substrate, substantiates the expected high efficiency possible with this material. Interestingly, a native oxide made by anodic oxidation in a liquid electrolyte has been shown to produce an acceptable single-layer AR coating on this cell. Excellent cell results have also been obtained with heterojunction InP/CdS epitaxial cells (14–15 percent AM2) and indium-tin-oxide/InP heterojunction cell (15 percent AM2), indicating that InP is an outstanding solar cell material.

Tin Oxide and Indium-Tin Oxide (ITO)

Wide bandgap semiconductors may be used as transparent front contacts and AR coatings combined in solar cells. Tin oxide, SnO_2, and indium oxide, In_2O_3, having about 9 percent tin doping and commonly identified as indium-tin oxide (ITO) have bandgaps near 4 eV and bulk resistivities as low as $2 \times 10^{-3}\ \Omega \cdot \text{cm}$, and so can function as transparent electrical conductors. They have been deposited on semiconductor substrates by spray pyrolysis, by chemical vapor deposition (CVD), and by ion beam sputtering. The oxides have indices of refraction around 2, and are typically deposited in layers about 750 Å thick if they are to be used as AR coatings, or up to several thousand angstroms thick when used as high-conductivity coatings alone. They may be used to increase conductivity of the front layer of a conventional *pn*-junction cell of Si, for example (Tanakura et al., 1980), or in SIS cells involving single-crystal or polycrystalline substrates, where AM1 efficiencies based on active areas of 16.2 percent and 11.2 percent, respectively, have been measured (Burk et al., 1980).

Polymer-Semiconductor Schottky-Barrier Cells $(SN)_x$/GaAs

The substance $(SN)_x$ is a metallic polymer that exhibits highly anisotropic electrical conduction. The material has a dc conductivity around 10^3 $(\Omega \cdot \text{cm})^{-1}$ along its polymer chains and 100 times lower conductivity perpendicular to the chains. It has been shown (Cohen and Harris, 1978) that barrier heights of $(SN)_x$ on various semiconductors are higher than those of elemental metals on the same semiconductors, leading to the realization of a Schottky-barrier cell of $(SN)_x$ on GaAs (with a thin gold layer for enhanced conductivity in the front of the cell) with an open-circuit voltage as high as 0.71 V. This contrasts with the V_{oc} of gold alone on GaAs of only 0.49 V. AM1 efficiencies in excess of 6 percent without use of an AR coating were obtained in the initial test of this material combination.

Use of the polymer, which has the band structure of a highly anisotropic

semimetal, appears simpler than that of the MIS approach (Sec. 11.3), which requires reliable formation of an insulating layer only 10 to 20 Å thick. To apply the $(SN)_x$ polymer, a bath of the polymer is heated in a vacuum until the material sublimes and condenses on the cooled substrate to form a layer of the desired thickness.

Organic Solar Cells

Although it is philosophically appealing to contemplate widespread use of solar cells made from thin films of organic substances such as chlorophyll, the problems seem formidable at present, and efficiencies achieved have mostly been well below 1 percent.

Organic films tend to have high but quite wavelength-dependent optical absorption coefficients, and they have high electrical resistivity, typically 10^5 to $10^8\ \Omega \cdot$ cm due to high trap densities, which lead to high series resistance, difficulty in making ohmic contacts, and space-charge limiting of current if the films are too thick.

If results to date seem disappointing it should be remembered that the efficiency with which all plants averaged together convert sunlight to biomass is only about 1 percent.

10.4 PROSPECTS FOR MASS-PRODUCED THIN-FILM CELLS

The diversity of the materials under investigation for use in thin-film cells is suggested by Table 10.3, from Barnett and Rothwarf (1980). In developing a scheme for planning material and cell development intelligently so as to reach the low-cost goals, those authors consider a generic thin-film cell structure (Fig. 10.5), divided into five functional regions;

- *Encapsulant and AR coating*. Typically the encapsulant may be glass to which the cell is attached, or a thin film of glass may be applied to the cell. The AR coating may involve layers to provide matching for transmission of light into the cell from the surrounding air, or structural alterations of the cell surface (texturing) to make the transition less abrupt.
- *Transparent contact*, which may be a conducting transparent (wide bandgap) semiconductor such as ITO or an open conducting grid—made of a material such as Ag, Ag/Ti/Pd mixtures, Au, graphite, Cu, or Ni—deposited either on the semiconductor absorber-generator layer beneath it or on the encapsulant, such as glass, if that is to be used as the supporting substrate for the entire cell.
- *Semiconductor absorber-generator* in which photons produce elec-

Table 10.3 Thin-film cell results reported for unconcentrated light

For sources of data see Barnett and Rothwarf (1980), Table 1 and References, except where noted

Absorber-generator/ collector-converter	Semiconductor thickness, 10^{-4} cm	Device area, cm^2	Absorber energy gap, eV	V_{oc}, V	J_{sc}, mA/cm^2	Fill factor	Efficiency, %	Illumination, mW/cm^2
Si/Si	25	9	1.1	.57	23.5	.72	9.5	AM1
$CuInSe_2$/CdS	1	1.2	1.04	.49	25	.54	6.6(10.6)*	100
Cu_2S/CdS	25	.9	1.2	.52	21.8	.71	9.15	88
CdTe/CdS	8	0.1	1.44	.75	14	.58	8.7(10.5)†	70
Cu_2S/ZnCdS	25	1.3	1.2	.57	19.2	.69	8.7	87
GaAs/I-M‡	25	9	1.43	.57	19.2	.60	6.5	AM1
InP/CdS	25	.25	1.3	.46	13.5	.68	5.7	74
a–Si/I-M‡	1	.02	1.6	.8	12	.58	5.6	65
a-Si/a-Si	1	1.09	1.6	.84	17.8	.676	10.1§	AM1
CdSe/ZnSe/Au	2	0.01	1.7	.60	20	.45	5.0	100
CuTe/CdTe	10	6	1.4	.59	13	.63	4.8	100
$CuInS_2/CuInS_2$	4	.12	1.55	.41	18.9	.43	3.33	100
ZnP_2/Mg	10	.0025	1.5	.43	13	.45	3.0	83
InSe/Bi	10	—	1.3	.35	3	.4	1.3	70
Cu_2C/Cu	250	1	2	.35	7	.45	1.1	100
Merocyanine/Al	5	1	2	1.2	1.8	.25	.7	—
CdSe/ZnTe	10	.1	1.7	.56	1.89	.48	.6	85

* Efficiency reported for $CuInSe_2$/(Cd, Zn)S cell. [Mickelsen, R. A., and Chen, W. S. (1982), Record, 16th IEEE Photovoltaic Spec. Conf., to be published.]

† Efficiency reported for CdTe/CdS cell having 4-μm-thick CdTe layer on 0.1-μm-thick CdS. [Tyan, Y. S., and Perez-Albuerne, E., (1982), Record, 16th IEEE Photovoltaic Spec. Conf., to be published.]

‡ Insulator-Metal (I-M)

§ Results for *p-i-n* a-Si:H cell having a-SiC:H window layer. [Catalano, A., et al., (1982), Record, 16th IEEE Photovoltaic Spec. Conf., to be published.]

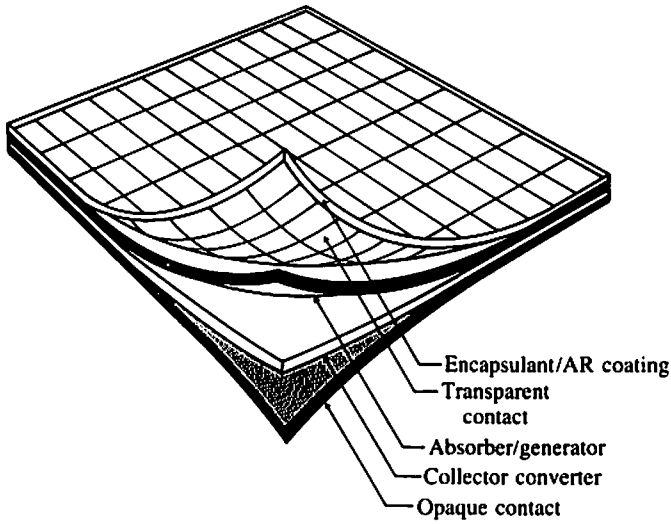


Figure 10.5 Exploded view of generic thin-film solar cell. (*Barnett and Rothwarf, 1980. © 1980 IEEE.*)

trons and holes. Requirements are a suitable energy gap and optical absorption coefficient, and a sufficiently long minority-carrier diffusion length to permit carriers to reach the collector-converter below the absorber-generator layer.

- *Semiconductor collector-converter* where minority carriers from the absorber-generator are converted to majority carriers, and which prevents the back flow of carriers. The built-in voltage between the absorber and collector regions serves as the barrier and determines how much voltage the cell can produce. This converter-collector layer must have a conductivity type opposite to that of the absorber-generator, and should have an electron affinity matching that of the absorber-generator to keep both the cell voltage and the cell current high. (*Electron affinity* is the energy required to raise an electron from the conduction band to the vacuum level, just outside the semiconductor surface.)
- *Opaque electrical contact of low resistivity.* The contact must make ohmic contact to the semiconductor collector-converter layer above it, for which it may serve as the substrate during growth of the layers of the cell. The contact is typically a thin metal such as copper or steel, and it may be required to have a high reflectivity for photons that reach it by passing through the cell without being absorbed.

Loss Mechanisms

Clearly with five distinct layers there are many possible cell materials to be considered, and it is not obvious how one should proceed in developing the

thin-film cell. Following Barnett and Rothwarf (1980), we will describe the losses that in real cells can reduce efficiencies below the theoretical levels of up to 24 percent shown in Fig. 10.1. We will then summarize their results on CdS/Cu_2S cell development and their conclusions regarding candidates for low-cost thin-film cells.

Optical losses These are of two types: 1) reflection losses and 2) extraneous, nonproductive absorption by layers or interfaces. Optical losses may range from 5 to 25 percent, of which extraneous absorption may account for 0 to 10 percent. Reflection losses at the several interfaces run from a minimum 5 percent to as much as 18 percent, occurring at the air-encapsulant boundary (0 to 3 percent), the transparent contact (shading, 5 to 10 percent; losses in a conducting oxide if one is used, 0 to 2 percent), semiconductor interfaces (0 to 5 percent), and at the opaque contact (<2 percent).

Electrical losses These divide naturally into three categories: (1) current losses, accounting for those minority carriers not collected and converted to majority carriers; (2) voltage losses, being the reduction of V_{oc} below the maximum voltage possible due to excitation of carriers to the conduction band in the absorber-generator semiconductor; and (3) resistance losses, due to series and shunt resistance and to a poor diode characteristic, all of which reduce the fill factor at the maximum power point.

In optimized cells, current losses due to carrier recombination in the bulk may range from 5 to 20 percent, surface recombination 0 to 5 percent, and recombination at grain boundaries from none in single-crystal cells to 5 percent. Current loss due to recombination at the interface in a heterojunction cell may be substantial. If there is a lattice mismatch of amount δa there, then the interface surface-state density is about $\delta a/a^3$ cm^{-2}, where a is the mean lattice spacing for the materials that meet at the interface. This surface-state density ranges from, say, 10^{10} cm^{-2} for a very good lattice match to 10^{14} cm^{-2} for a few percent misfit. For example, in the CdS/Cu_2S cell one has a surface recombination velocity around 10^5 cm/s with a 4 percent lattice misfit. The net carrier loss due to the interface recombination might be less than 5 percent in optimized material, or as high as 30 to 40 percent in nonoptimized material.

Voltage losses are controlled in *pn*-junction and Schottky-barrier cells by the factors determining V_{oc}, namely either bulk recombination lifetime or interface and surface recombination rates, as well as the energy gap and dopant levels on opposite sides of the junction. These losses for modest doping levels may run from 4 to 50 percent. At heavy doping levels, bandgap narrowing, degeneracy effects, and Auger recombination add to the voltage losses.

Series resistance losses result from current flow over resistive paths in the

front layer of the *pn*-junction cell, and so depend on the grid spacing, the thickness of the layer, and the presence of any defects that scatter carriers in that layer. Finite shunt resistance may arise from surface leakage across the junction or conducting paths produced by diffusion of dopants along grain boundaries, or possibly by tunnelling through the junction where there is an inhomogeneous doping that concentrates the electric field.

Losses due to degradation processes One would like cells to function well for 20 years, at 80 to 90 percent of their initial efficiency. Outputs may fall gradually below their initial values for several reasons. Dust and dirt accumulate, but can be removed periodically. Irreversible intrinsic degradation processes include unwanted diffusion of contact materials or dopants, especially along grain boundaries, and possibly even electromigration of material in regions where the current density is high. Extrinsic processes include oxidation of semiconductor layers if the encapsulant is breached, contact or AR coating deterioration, darkening of encapsulant due to UV exposure or weathering, and the effects of extreme temperature cycling while the cell is in use. Partial shading of a series-connected array can destroy the shaded cells, which are reverse-biased by voltage from the illuminated cells, if the cells are not provided with protective diodes.

Increasing Efficiency of Thin-Film Cells

Analysis and gradual reduction of the losses in CdS/Cu_2S thin-film cells over a five-year period led to an increase in typical laboratory efficiencies from around 5 or 6 percent to values of 9 percent by 1980. The changes made included reducing reflection from the metallic front contact by use of an evaporated contact, use of a silicon dioxide encapsulant instead of mylar and epoxy (further work is still needed on encapsulants that keep oxygen from the Cu_2S), hydrogen heat treatment to reduce recombination losses in the Cu_2S absorber-generator by improving stoichiometry, as well as heat treatments to reduce shunt resistance losses. It is expected that further development based on loss analysis will permit realizing cells having 10 percent efficiencies, with an ultimate goal of an optimized CdS/Cu_2S cell having 11.6 percent AM1 efficiency (Barnett and Rothwarf, 1980). For that cell expected characteristics are $V_{oc} \sim 0.57$ V, $J_{sc} \sim 27$ mA/cm^2, and a fill factor around 0.75.

The electron affinity match between absorber and collector can be improved by substituting 20 to 30 percent Zn for Cd in the CdS collector-converter, and so reducing the loss of open-circuit voltage occurring at the absorber-collector Cu_2S-CdS junction. An 8.7 percent efficiency has been reported for this zinc-substituted (CdZn)S/Cu_2S cell, and an optimized efficiency of 15 percent is anticipated (Barnett and Rothwarf, 1980).

Cost Estimates for Production Thin-Film Cells

The cost of producing thin-film CdS/Cu_2S cells by the continuous processing line shown schematically in Fig. 10.6 has been analyzed both by methods familiar to chemical engineers and with the SAMICS methodology (Appendix 7). Results are listed in Table 10.4 for CdS/Cu_2S, and cost estimates obtained by using similar methods for many other thin-film material systems appear in Table 10.5.

The hypothetical CdS plant, scaled-up from current laboratory processing, forms the 4-μm-thick CdS or CdZnS collector-converter by vacuum evaporation on the metallic 25-μm-thick Cu:Zn alloy substrate and back contact. Copper chloride is vapor-deposited and heated to form Cu_2S, the transparent contact is printed, and the 5-μm-thick glass encapsulant is sprayed on.

The cells are assumed to average 10 percent efficiency and the plant is assumed to have a 90 percent yield. The total estimated production cost is \$0.18/W_{pk}, of which 32 percent is material cost and 25 percent is labor cost. General and administrative costs account for about one-third, and the cost of capital for the 100-MW_{pk}/year plant amounts to about one-tenth of the final production cost. If the selling price for this large-volume item were 25 percent above the production cost, the price would be just \$0.23/W_{pk}.

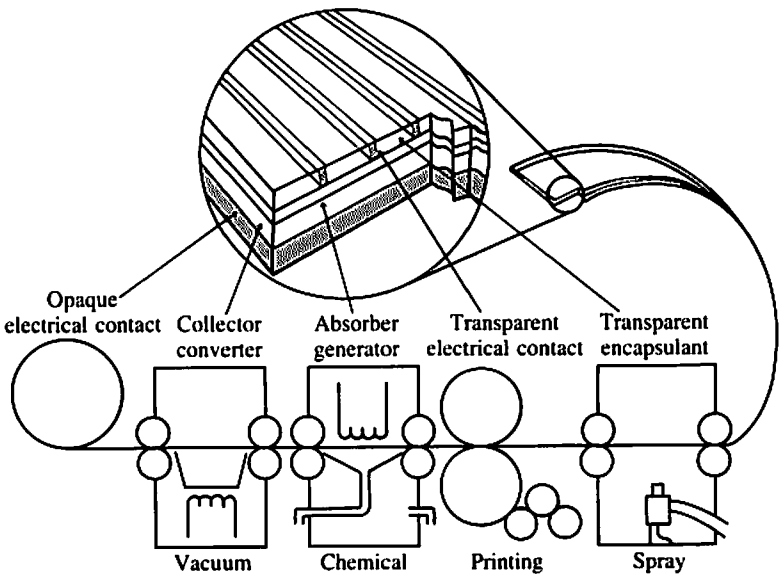


Figure 10.6 Schematic diagram of hypothetical continuous production process for making thin-film solar cells. (*Barnett and Rothwarf, 1980. © 1980 IEEE.*)

Table 10.4 Estimated costs of producing Cu_2S/CdS thin-film cells in a continuous automated factory (in U.S. \$/100 W_{pk})
See text for assumptions made. (Barnett and Rothwarf, 1980).

	Material	Production labor	Capital	General and administrative	Total
Opaque electrical contact (substrate of 25-μm-thick Cu:Zn alloy film)	3.150	.325	.065	1.520	5.060
Collector-converter (vacuum deposition of 4 μm of CdS or CdZnS)	.858	1.950	.839	1.730	5.377
Absorber-generator (vapor deposition of CuCl plus heater treatment)	.143	.955	.452	.747	2.297
Transparent electrical contact (printing of metallic grid)	1.144	.650	.194	.900	2.888
Encapsulation (spray deposition of 5-μm-thick glass compound)	.572	.650	.452	.768	2.442
TOTALS	5.867 (32.5%)	4.535 (25.1%)	2.002 (11.1%)	5.665 (31.3%)	18.064

The semiconductor materials (absorber, collector) in the cell just described contribute direct material costs of only \$0.01/W_{pk}. The other materials whose costs are given in Table 10.5 are listed in three categories based on semiconductor material costs (\$0.01/W_{pk} or less, above \$0.01 but less than \$0.20/W_{pk}, and \$0.20/W_{pk} or more). Thickness of the absorber-generator semiconductor is assumed to be 5 μm, like that in the CdS cells, except in cases where the optical absorption coefficients permit or require thinner or thicker layers. The same assumptions of 10 percent AM1 efficiency and 90 percent yield have been made.

Although there is certainly room for discussion regarding assumptions made about efficiency and costs, one cannot help but be encouraged by the existence of so many different material systems. It appears that thin-film solar cells with manufacturing costs as low as \$0.20/W_{pk} may be feasible.

10.5 SUMMARY

One expects that thin films of amorphous and polycrystalline semiconductors will be used increasingly in solar cells. Amorphous silicon cells are poten-

Table 10.5 Estimated costs and selling prices of various candidate thin-film cells made in continuous production processes
Assumptions are same as for Table 10.4 except where noted. (Barnett and Rothwarf, 1980)

Material system	Thickness, μm	Material cost, \$/watt	Manufacturing cost,* \$/watt	Selling price,† \$/watt
		Category 1		
Cu_2S/CdS	5	.01	.181	.226
Cu_2S/ZnCdS	5	.01	.181	.226
a–Si/I-M	5	.01	.181	.226
Cu_2O/Cu	5	.01	.181	.226
Zn_3P_2/Mg	5	.01	.181	.226
Merocyanine/Al	.5	.01	.181	.226
		Category 2		
Silicon	25	.03	.209	.261
CdTe/CdS	5	.03	.209	.261
Cu_2Te/CdTe	5	.03	.209	.261
CdSe/ZnTe	5	.04	.224	.280
InP/CdS	1	.06	.252	.315
		Category 3		
Silicon	200	.25	.522	.653
$CuInSe_2$/CdS	5	.20	.451	.564
GaAs/I-M	5	1.00	1.587	1.984
GaAs/I-M	1	.20	.451	.564
InP/CdS	5	.30	.593	.741

* Non-semiconductor material costs are \$0.167/watt for continuous process with thin-film encapsulant and opaque contact. Semiconductor material costs are increased by 42% for research, selling, and distribution charges and are assumed at 80% yield.

† Assumes 25% mark-up over manufacturing costs.

Note: I-M = Insulator-metal

Category 1 < \$.01/watt
Category 2 < \$.03 to \$.06/watt
Category 3 < \$.20 to \$1.00/watt

tially quite inexpensive, and have demonstrated an efficiency slightly above 10 percent. Prospects appear good for achieving large-scale production of thin-film cells costing \$0.30/W_{pk} or less. A number of candidate materials exist, including CdS/Cu_2S, a partially zinc-substituted CdZnS/Cu_2S, and InP/CdS.

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PROBLEMS

10.1 *Semiconductor properties and cell performance* Referring to Table 10.1 and Ch. 3, answer the following:

(*a*) As energy gap varies, how does the portion of the spectrum that is effective vary?

(*b*) Why does the minority carrier diffusion length affect collection efficiency?

(*c*) What type of semiconductor should be chosen in order to use the least amount of semiconducting material in a cell?

(*d*) How does carrier mobility affect the series resistance of a cell?

(*e*) If one uses a polycrystalline rather than a single-crystal form of a given semiconductor, which of the following properties are likely to be altered: size and type of energy gap, minority carrier lifetime, minority carrier diffusion length, conductivity types that are possible, carrier mobility?

(*f*) Why is minority carrier lifetime likely to be small in a direct-gap material?

(*g*) What constraints on cell processing does the use of a direct-gap material impose?

10.2 *Single wavelength cell* How might a photodiode designed for operation at a single photon energy, such as 1.5 eV, differ from a well-designed solar cell for use in sunlight?

10.3 *The best thin-film material* If, on behalf of a government-sponsored, long-term research program, you were to choose one or two thin-film cells for further research, which would you choose? Explain your choice and compare it (them) with the best competitors.

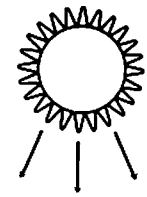
10.4 *Two decades from now* What are your views of the prospects, in the next 20 years, of silicon solar cells versus non-silicon cells and thin-film cells versus single crystal cells? Will they coexist or will one type dominate? Explain your reasoning.

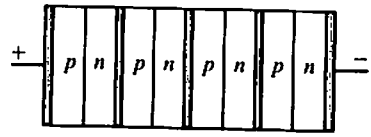
CHAPTER

ELEVEN

VARIATIONS IN CELL STRUCTURES

CHAPTER OUTLINE





Several different cell structures have been touched upon so far in the book. These will be briefly reviewed in Sec. 11.1. The discussion will then be expanded to include other variations. We shall make no attempt to review exhaustively the large number of known novel structures nor to establish their original sources. Rather, we shall try to examine the different approaches by which to improve cell performance. Not surprisingly, the more complex cell structures have all been proposed for concentrator systems, in which high unit-area cell costs can be tolerated (see Sec. 5.2).

11.1 REVIEW OF SOME BASIC STRUCTURES

Conventional Homojunction Cell

This is the simplest structure, consisting of a *pn* junction in a single semiconductor (see Chap. 3) parallel to the surface with finger electrodes on the front surface. For materials such as Si and GaAs, in which high-quality homojunctions can be formed easily, this structure probably provides the best combination of simple fabrication and high performance.

Heterojunction Cell

Here the *pn* junction is formed by two different materials. The best example is the solar cell based on CdS, for which no reliable technology for making homojunctions exists. Instead, *n*-type CdS film is dipped in a hot $CuCl_2$ solution, or otherwise a layer of Cu_2S, which is naturally *p*-type, is deposited on the CdS film (see Fig. 7.3). Another example is the ITO (indium-tin-oxide) on Si heterojunction cell. Here the advantage is the transparency of the top semiconductor and the consequent elimination of recombination loss at the upper surface of the cell.

Schottky-Barrier (-Junction) Cell

A Schottky junction is a natural choice when *pn* junctions are difficult to make, such as in amorphous Si. The Schottky-junction structure is also popular among thin-film polycrystalline Si or GaAs cells, for which there is some fear of junction shorts due to rapid diffusion along grain boundaries. The technological challenge is to find suitable metals or surface treatments to make the reverse saturation current I_0 as low as or lower than that of *pn*-junction cells. Large I_0 translates into low open-circuit voltage V_{oc} and efficiency η. Deposition of metals thin enough for light transmission and thick enough for good electrical conductance also requires care.

11.2 UNCONVENTIONAL NONCONCENTRATOR CELLS

These cell structures were not proposed specifically for concentrator systems, although they or variations of them could also find use as concentrator cells.

Metal-Insulator-Semiconductor (MIS) Cells

As stated earlier, Schottky-junction cells tend to have high reverse saturation current, I_0. It is reasonable that I_0 could be reduced by adding an additional energy barrier—an insulator layer between metal and semiconductor. The insulator layer unfortunately can be expected to cut down the short-circuit current by hindering the carrier flow, too. The net effect is an increase in cell efficiency if the insulator is some 10 to 20 Å thick. Figure 11.1 illustrates these facts (Card, 1976).

Rather complex theories and experiments have been presented for MIS cells (Shewchun, 1980). The physical processes are still not entirely clear and the technology is under investigation.

Induced-Junction Cells

It was pointed out in Chap. 3 that it is usually desirable to reduce the thickness of the top layer of a *pn*-junction cell to avoid the recombination loss at the front surface. The ultimate shallow junction may be that of an inversion layer

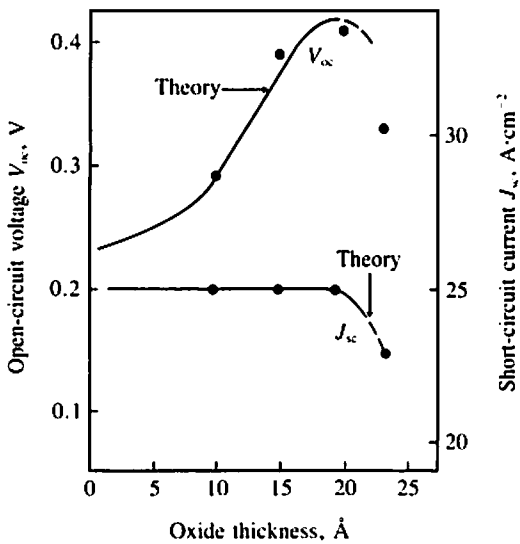


Figure 11.1 In a MIS cell, the thin insulator (oxide) between the metal and semiconductor raises V_{oc} without significantly reducing J_{sc}. Thus, adding the insulator layer improves the cell efficiency. (*Card, 1976.*)

on the surface of bulk semiconductor (Call, 1973). An n-type inversion layer may be induced by a positively biased field plate, as in an MOS field-effect transistor, or by positive charges deliberately introduced in the insulator, or both. Figure 11.2 shows an induced-junction cell with a transparent field plate. Notice that no power is consumed by biasing the field plate since no current flows through the SiO_2 insulator.

Discontinuous-Junction Cells

The *pn* or Schottky junction of a solar cell does not have to cover the entire cell surface. The junction may take the form of thin stripes or even a matrix of small dots and still collect carriers efficiently if the spacing between junctions is small compared to a diffusion length. For Schottky-junction cells, this is expected to decrease the reverse saturation current (smaller junction area at the same saturation current density) and hence raise efficiency (Green, 1975). For *pn* junctions, this will have little effect on the reverse saturation current (Hu, 1977), but may increase the short-circuit current slightly due to reduction of recombination in the diffused regions (Loferski, 1972).

Tandem-Junction Cell and Front-Surface-Field Cell

A cell can have *pn* junctions on both the illuminated and most of the unilluminated side (n^+pn^+ structure). Contacts are made to the p-type bulk from the back side through openings in the n^+ layer. This is called the *tandem junction cell*. In one mode of operation, the front and back n^+ regions are electrically connected. Expectedly, this structure provides a higher collection efficiency than the conventional structure, which collects carriers only at the front junction. Somewhat unexpectedly, the collection efficiency is also good when the front junction is left open. This can be explained by the fact that an

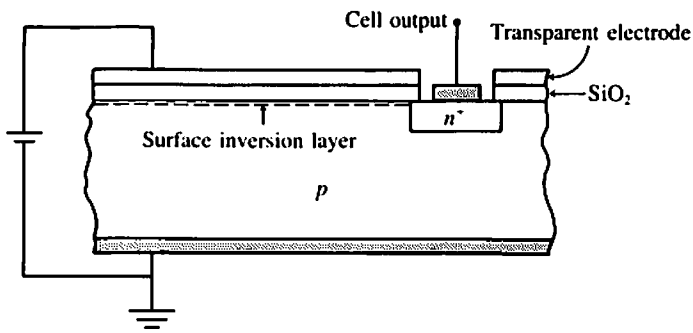


Figure 11.2 Induced junction cell. The field-induced surface inversion layer is the ultimate shallow n^+ layer. No current, therefore no power, is drawn from the biasing battery.

open-circuited n^+p junction effectively provides a low recombination velocity surface for the front side of the cell (Kim, 1980). A variation is to replace the front n^+p junction with a p^+p junction. This p^+pn^+ structure is called the *front-surface-field cell* because of its similarity, both in structure and operation, to the back-surface-field cell (Sec. 3.8). Both the open-circuited n^+p junction and the p^+p junction provide an effective low recombination surface. These cells, then, are basically the same as the interdigitated-back-contact cell discussed in Sec. 11.3.

Multiple-Pass Cells

In thin solar cells made of indirect-gap materials such as Si, it would be desirable to have sunlight make more than a single pass through the cell so as to achieve more complete light absorption. This can be done by plating the back surface with highly reflective metals (Muller, 1978). The path length can be further increased by texturing the front and/or back cell surface (see Fig. 4.8).

Liquid-Junction Cells

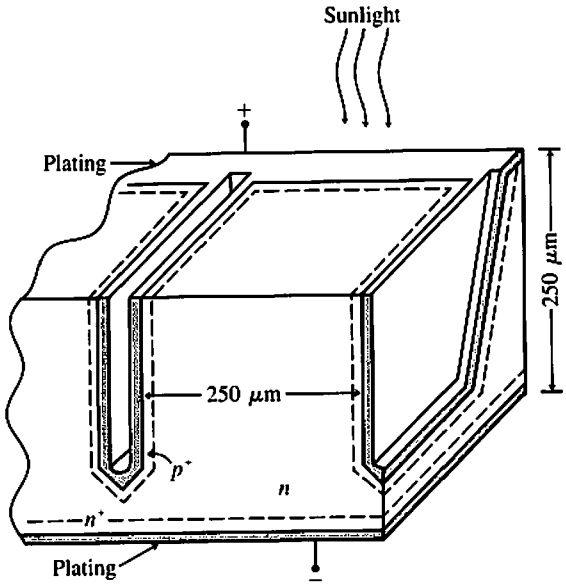
As an alternative to *pn* and Schottky junctions, an electrolyte/semiconductor junction can provide the built-in potential for the solar cell. The physics and chemistry of the liquid junction are less understood than for the *pn* junction, but the electrical behaviors of the liquid junction cells both in the dark and in the light are remarkably similar to those of more conventional cells. The technological challenge is to prevent corrosion of the semiconductor. Bell Laboratories have developed a cell (*Electronics*, 1981) with single-crystal indium phosphide photocathode in a solution that uses vanadium dichloride and vanadium trichloride as the ion couple in aqueous hydrochloric acid. Light shines on the p-type indium phosphide. Electrons diffuse to the surface, where they reduce the solution. The electrolyte, a metal anode, and the external load complete the circuit. This cell has a 11.5 percent efficiency.

One potential advantage of liquid junction cells is low cost, provided that a thin polycrystalline semiconductor is used. The electrolyte/semiconductor junction is also the building block of some photoelectrolytic cells to be discussed in Chap. 12.

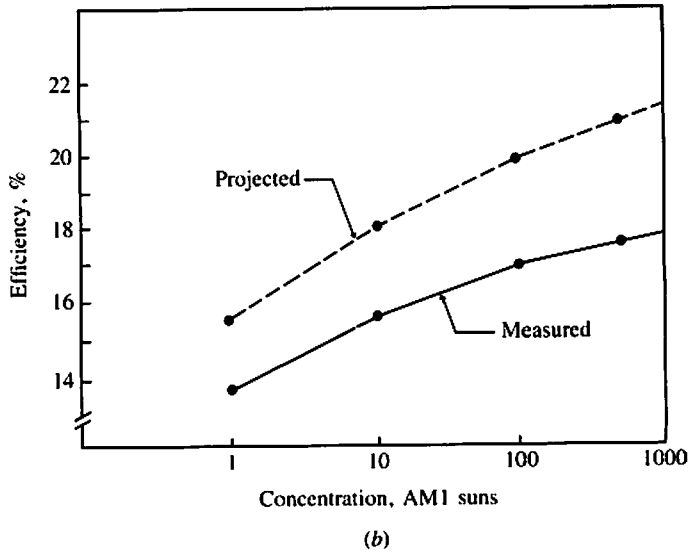
11.3 UNCONVENTIONAL CONCENTRATOR CELLS

Parallel Multiple-Vertical-Junction Cell

The concept of using closely spaced multiple vertical junctions originated from the desire to maintain good collection efficiencies in satellite-mounted



(*a*)



(*b*)

Figure 11.3 (*a*) A cell having multiple vertical junctions connected in parallel. (*b*) Measured efficiency and projected efficiency after certain improvements. Efficiency increases with the concentration ratio up to 1000 suns because of very low series resistance. (*Frank, 1980.*)